Professional high-speed optical transceiver

OPN-XS151-40LC2

8.5Gbps / 40 km / CWDM XFP Single-Mode Optical Transceiver for 8G FC Applications

PRODUCT FEATURES

- Up to 8.5 Gb/s Bi-directional Data Link
- Complaint with XFP MSA
- Compliant with Fiber Channel FC-PI-4 800-SN-LL-I
- Compliant with 4G, 2G Fiber Channel
- SFF-8472 Digital Diagnostic Function
- Maximum Link Length of 40 km
- Temperature-stabilized 8-Wavelength CWDM EMLTransmitter: from 1470 nm to 1610 nm
- 15 dB Power Budget at Least
- AC/AC Coupling according to MSA
- 2-Wire Interface for Integrated Digital DiagnosticMonitoring
- XFI Loopback Mode
- No reference Clock required
- Power Dissipation < 3.5 W
- +3.3 V & 5V Power Supply
- RoHS Compliant
- 0 to 70ºC Operating
- Duplex LC Connector

APPLICATIONS

- Multi-rate 8x/4x/2x Fibre Channel

STANDARD

- Compliant with XFP MSA
- Compliant with 8GFC

PRODUCT DESCRIPTION

OPN-XS151-40LC2 series multi-rate 8G XFPtransceivers are designed for serial optical data communications such as 8G Fibre Channel. It supports the8.5Gbps transmission on 9/125 μm SMF.

The transceiver consists of two sections: The transmittersection consists of a CWDM electrical-modulated laser (EML), driver and signal conditioner. The receiver sectionincorporates a PIN photodiode integrated with a trans-impedance preamplifier (TIA) and signal conditioner.There are eight center wavelengths available from 1470 nmto 1610 nm, with each step 20 nm. A guaranteed minimumoptical link budget of 15 dB is offered.

The module is with the XFP 30-pin connector to allow hot plug capability. Integrated Tx and Rx signal conditioners provide high jitter-tolerance for full XFI compliance and noexternal reference clock required. The internally ac coupledhigh speed serial I/O simplifies interfacing to externalcircuitry. Dual 5V and 3.3V power supply is needed. The optical output can be disabled by LVTTL logic high-level input of TX_DIS. Loss of signal (RX_LOS) output isprovided to indicate the loss of an input optical signal of receiver.

A serial EEPROM in the transceiver allows the user to access transceiver digital diagnostic monitoring and configuration data via the 2-wire XFP Management Interface. This interface uses a single address, A0h, with amemory map divided into a lower and upper area. Basic digital diagnostic data is held in the lower area while specificdata is held in a series of tables in the high memory area.

ORDER INFORMATION

P/No.	Bit Rate (Gb/s)	FC-PI	Power Budget (dB)	Wavelength (nm)	Package	Case Temp (ºC)	RoHS Compliant
OPN-XS151-40LC2	8 /4 /2	FC-PI-4	>15	CWDM*	XFP with DMI	0 to 70	Yes

CWDM* Wavelength (0 to 70ºC)

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Central Wavelength	Min.(nm)	Typ.(nm)	Max.(nm)	Central Wavelength	Min.(nm)	Typ.(nm)	Max.(nm)
147	1464.5	1470	1477.5	155	1544.5	1550	1557.5
149	1484.5	1490	1497.5	157	1564.5	1570	1577.5
151	1504.5	1510	1517.5	159	1584.5	1590	1597.5
153	1524.5	1530	1537.5	161	1604.5	1610	1617.5

CWDM*: 8 Wavelengths from 1470 nm to 1610 nm, each step 20 nm.

Absolute Maximum Ratings					
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Notes**
Storage Temperature	Tstg	-50	85	°C	
Operating Case Temperature	Topr	0	70	°C	
Relative Humidity	RH	0	85	%	Non condensing
Power Supply Voltage (5V)	Vcc5	-0.5	3.6	V	
Power Supply Voltage (3.3V)	$V_{CC}3$	-0.5	3.6	V	
Receiver Input Optical Power	Mip		4	dBm	Received average power

Recommended Operating Conditions					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units / Notes**
Power Supply Voltage (5V)	$V_{CC}5$	4.75	5	5.25	V
Power Supply Voltage (3.3V)	$V_{CC}3$	3.13	3.3	3.47	V
Power Supply Current (@5V)	$I_{CC}5$			500	mA / 1
Power Supply Current (@3.3V)	$I_{CC}3$			750	mA / 1
Power Dissipation	P_D			3.5	W
Operating Case Temperature	Topr	0		70	°C
Data Rate			8.5		Gb/s

1. Including in rush current. Maximum module current ramp rate is 100 mA/μs.

Transmitter Optical Specifications (Topr= 0 to 70°C, Vcc5=5V±5%, Vcc3 = 3.3V ±5%)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Average Launch Power	$Po_{, Avg}$	-1		+4	dBm	2
Extinction Ratio	ER	8.2			dB	
Output Center Wavelength	λc	λc –5.5	λc	λc +7.5	nm	3
Output Spectrum Width	σ_λ			1	nm	-20 dB width
Side Mode Suppression Ratio	SMSR	30			dB	
Relative Intensity Noise	RIN			-130	dB/Hz	
Average Launch Power of OFF Transmitter				-30	dBm	

2. Output power is power coupled into a 9/125 μm single-mode fiber.
3. ITU-T G.694.2 CWDM wavelength from 1470 nm to 1610 nm, each step 20 nm.

Receiver Optical Specifications (Topr= 0 to 70°C, Vcc5=5V±5%,Vcc3 = 3.3V ±5%)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Sensitivity	Sen1			-16	dBm	4
Receiver Overload	P_{MAX}	-1	---		dBm	
LOS -- Deasserted	LOS_D	---	---	-22	dBm	Transition: low to high
LOS -- Asserted	LOS_A	-28	---	---	dBm	Transition: high to low
LOS -- Hysteresis		0.5	---		dB	
Wavelength of Operation	λc	1260		1620	nm	
Optical Return Loss	ORL			-27	dB	

4. Average received power; BER < 10^{-12} and PRBS 2^7-1

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Electrical Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
High-Speed Signal (CML) Interface Specification						
Input Data Rate			8.5		Gb/s	
TX Clock Tolerance				±100	ppm	1
Differential Input Impedance	Rin		100		Ω	
Differential Data Input Amplitude		120		820	mVpp	2, Internally AC coupled
Output Data Rate			8.5		Gb/s	
RX Clock Tolerance				±100	ppm	1
Differential Output Impedance	Rout		100		Ω	
Differential Data Output Amplitude		340		850	mVpp	2, Internally AC coupled
Low-Speed Signal (LVTTL) Interface Specification						
Input High Voltage		2.0		Vcc	V	
Input Low Voltage		GND		0.8	V	
Output High Voltage		2.4		Vcc	V	
Output Low Voltage		GND		0.5	V	
Reference Clock (LVPECL) Interface Specification						
No reference clock						

1. Clock tolerance for 8.5Gb/s, 4.25Gb/s, 1.063Gb/s and 1.25Gb/s
2. The differential input and output amplitudes are per XFP MSA mask at points B' and C'.

Transceiver Timing Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
TX_DIS Assert Time	t_off			10	s	
TX_DIS Negate Time	t_on			2	ms	
Time to Initialize	t_init			300	ms	
Interrupt Assert Delay	interrupt_on			200	ms	
Interrupt Negate Delay	interrupt_off			500	s	
P_Down/PST Assert Delay	P_Down/RST_on			100	s	
P_Down Nagate Delay	P_Down/RST_off			300	ms	
Mod_NR Assert Delay	Mod_nr_on			1	ms	
Mod_NR Negate Delay	Mod_nr_off			1	ms	
Mod_Desel Assert Time	T_Mod_Desel			2	ms	
Mod_Desel De-Assert Time	T_Mod_Sel			2	ms	
P_Down Reset Time	T_reset	10			s	
RX_LOS Assert Delay	T_Los_on			100	s	
RX_LOS Negate Delay	T_Los_off			100	s	
Serial ID Clock Rate	f_{SCL}	0		400	kHz	

MANAGEMENT INTERFACE

The structure of the memory map is shown in Figure 1, which is accessible over a 2-wire serial interface at the 8-bit address 1010000X (A0h). The normal 256 byte I2C address space is divided into low and upper blocks of 128 Bytes. The lower block of 128 Bytes is always directly available and is used for the diagnostics and control function. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. Thus, there is a total available address space of 128*256 = 32 Kbytes in this upper memory space. The contents of Table 01h are listed in Table 1 below. Please refer SFF INF-8077i (Revision 4.5) for detailed information.

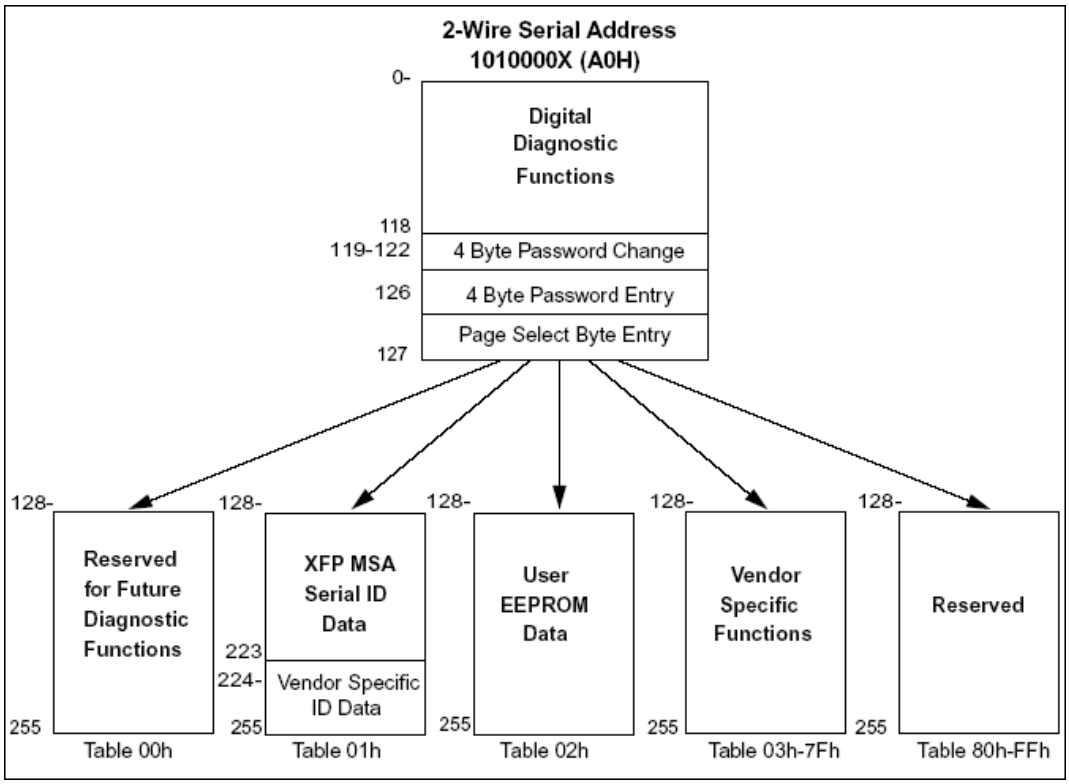

Figure 1. 2-wire Serial Digital Diagnostic Memory Map

Table 1 Monitoring Specification

Data Address	Parameter	Accuracy
96 ~ 97	Temperature	± 3ºC
98 ~ 99	Reserved	
100 ~ 101	Tx Bias	± 10%
102 ~ 103	Tx Power	± 2dB
104 ~ 105	Rx Power	± 2dB
106 ~ 107	Vcc3	± 3%

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CONNECTION DIAGRAM

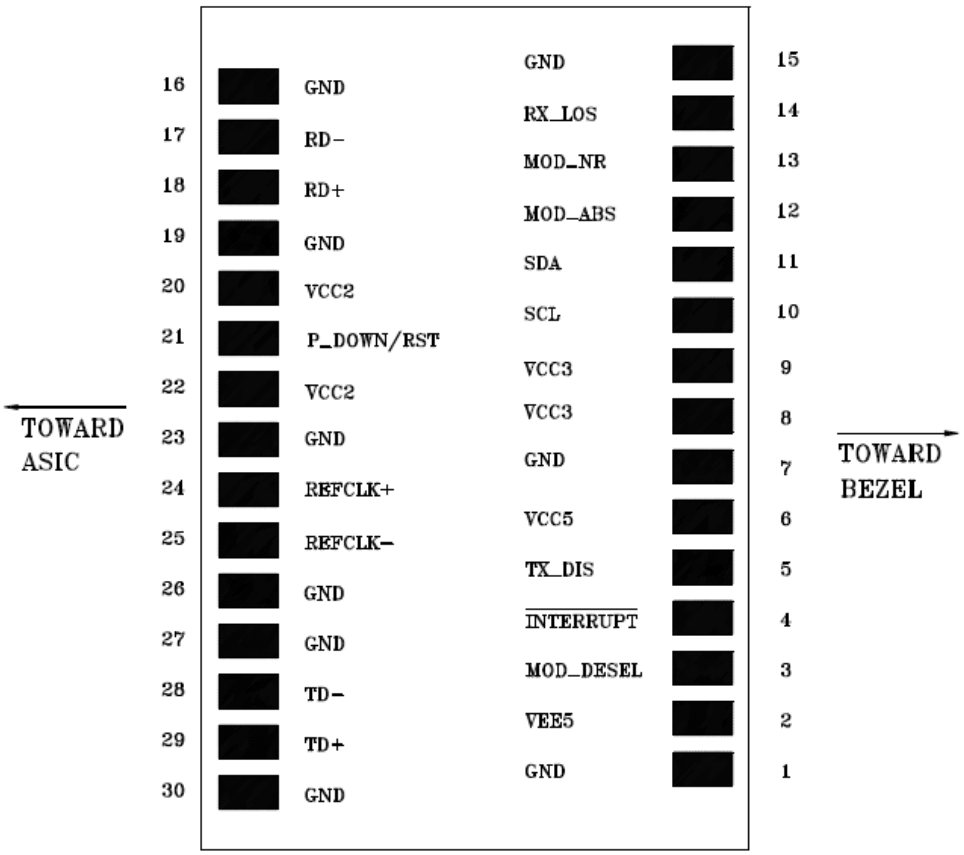


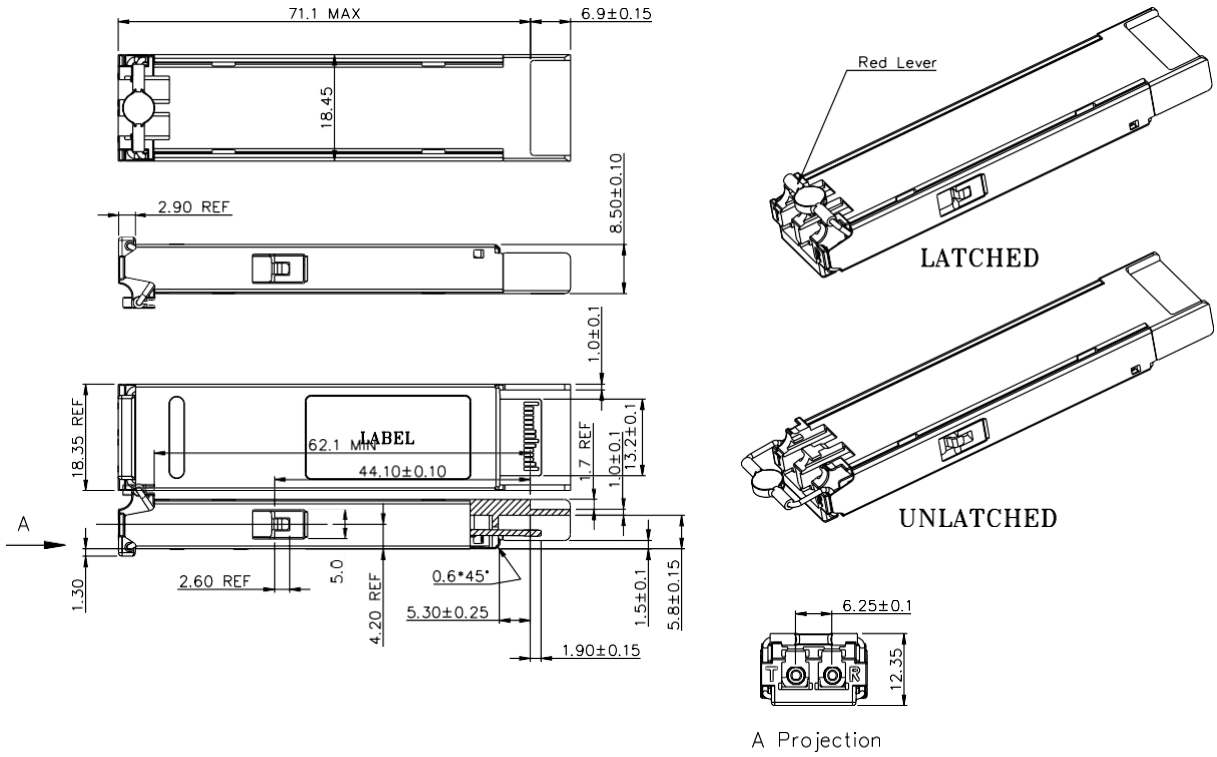
Table 3 PIN Description

PIN	Logic	Signal Name	Description	Note
1		GND	Module Ground	1
2		VEE5	-5.2V Power Supply **(Not required)**	3
3	LVTTL-I	Mod_Desel	Module De-select; When held low allows module to respond to 2-wire serial interface	
4	LVTTL-O	$\overline{\text{Interrupt}}$	Interrupt; Indicates presence of an important condition which can be read over the 2wire serial interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Turns off transmitter laser output	
6		VCC5	+5V Power Supply	3
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I/O	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Indicates Module is not present. Grounded in the Module	2
13	LVTTL-O	Mod_NR	Module Not Ready; Indicating Module Operational Fault	2
14	LVTTL-O	RX_LOS	Receiver Loss Of Signal Indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver Inverted Data Output	
18	CML-O	RD+	Receiver Non-Inverted Data Output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply **(Not required)**	3

21	LVTTL-I	P_Down/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode. Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply **(Not required)**	3
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock Non-Inverted Input, AC coupled on the host board. **(Not used. Internally terminated to 50 ohm (100 ohm diff.))**	4
25	PECL-I	RefCLK-	Reference Clock Inverted Input, AC coupled on the host board. **(Not used. Internally terminated to 50 ohm (100 ohm diff.))**	4
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter Inverted Data Input	
29	CML-I	TD+	Transmitter Non-Inverted Data Input	
30		GND	Module Ground	1

1. Module ground pins GND are isolated from the module case and chassis ground within the module.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.
3. These PINs are open within module.
4. A Reference Clock input is not required. If present, it will be ignored.

MECHANICAL SPECIFICATION (UNITS IN MM)



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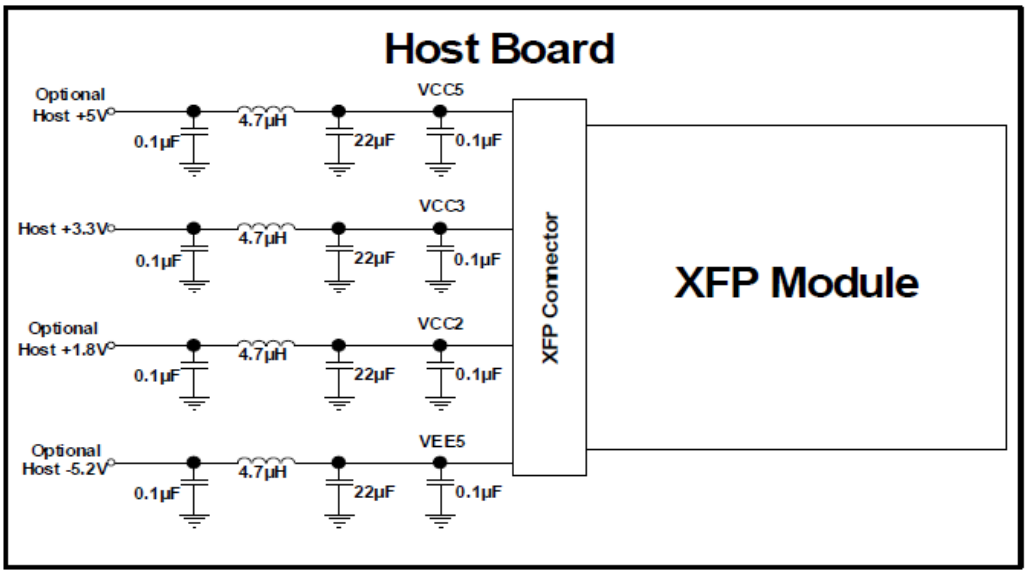
RECOMMENDED POWER CIRCUIT SCHEMATIC



RECOMMENDED INTERFACE CIRCUIT