

## Professional high-speed optical transceiver

### OPN-XS135-40LC2

3.3V / CWDM / 8.5Gbps XFP Single-Mode Optical Transceiver for 8G FC Applications

#### PRODUCT FEATURES

- Up to 8.5 Gb/s Bi-directional Data Link
  - Complaint with XFP MSA
- Compliant with Fiber Channel FC-PI-4 800-SN-LL-I
  - Compliant with 4G, 2G Fiber Channel
  - SFF-8472 Digital Diagnostic Function
- 8-Wavelength ( $\lambda$ ):1350 nm to 1410 nm CWDM DFB LDTransmitter
  - Distance up to 40km
  - AC/AC Coupling according to MSA
- 2-Wire Interface for Integrated Digital DiagnosticMonitoring
  - XFI Loopback Mode
  - No reference Clock required
  - Power Dissipation < 2 W
- Only Required +3.3 V Power Supply
  - RoHS Compliant
  - 0 to 70°C Operating
  - Duplex LC Connector

#### APPLICATIONS

- Multi-rate 8x/4x/2x Fibre Channel

#### STANDARD

- Compliant with XFP MSA
- Compliant with 8GFC

#### PRODUCT DESCRIPTION

OPN-XS135-40LC2 series multi-rate 8G XFPtransceivers are designed for serial optical data communications such as 8G Fibre Channel. It supports the8.5Gbps transmission on 9/125  $\mu$ m SMF.

The transceiver consists of two sections: The transmittersection consists of a directly modulated CWDM multiple quantum well DFB laser, driver and signal conditioner. Thereceiver section incorporates a PIN photodiode integratedwith a trans-impedance preamplifier (TIA) and signalconditioner. There are eight center wavelengths availablefrom 1350 nm to 1410 nm, with each step 20 nm. Aguaranteed minimum optical link budget of 16 dB is offered.The module is with the XFP 30-pin connector to allow hot plug capability. Integrated Tx and Rx signal conditionersprovide high jitter-tolerance for full XFI compliance and noexternal reference clock required. The internally ac coupledhigh speed serial I/O simplifies interfacing to externalcircuitry. Dual 5V and 3.3V power supply is needed. Theoptical output can be disabled by LVTTTL logic high-levelinput of TX\_DIS. Loss of signal (RX\_LOS) output isprovided to indicate the loss of an input optical signal of receiver.

A serial EEPROM in the transceiver allows the user to access transceiver digital diagnostic monitoring and configuration data via the 2-wire XFP Management Interface. This interface uses a single address, A0h, with a memory map divided into a lower and upper area. Basic digital diagnostic data is held in the lower area while specificdata is held in a series of tables in the high memory area.

#### ORDER INFORMATION

| P/No.           | Bit Rate (Gb/s) | FC-PI   | Power Budget (dB) | Wavelength (nm) | Package      | Case Temp (°C) | RoHS Compliant |
|-----------------|-----------------|---------|-------------------|-----------------|--------------|----------------|----------------|
| OPN-XS135-40LC2 | 8 / 4 / 2       | FC-PI-4 | >16               | CWDM*           | XFP with DMI | 0 to 70        | Yes            |

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CWDM\* Wavelength (0 to 70°C)

| Central Wavelength | Min.(nm) | Typ.(nm) | Max.(nm) | Central Wavelength | Min.(nm) | Typ.(nm) | Max.(nm) |
|--------------------|----------|----------|----------|--------------------|----------|----------|----------|
| 127                | 1264.5   | 1270     | 1277.5   | 135                | 1344.5   | 1350     | 1357.5   |
| 129                | 1284.5   | 1290     | 1297.5   | 137                | 1364.5   | 1370     | 1377.5   |
| 131                | 1304.5   | 1310     | 1317.5   | 139                | 1384.5   | 1390     | 1397.5   |
| 133                | 1324.5   | 1330     | 1337.5   | 141                | 1404.5   | 1410     | 1417.5   |

CWDM\*: 8 Wavelengths from 1350 nm to 1410 nm, each step 20 nm.

### Absolute Maximum Ratings

| Parameter                  | Symbol           | Min | Max              | Units | Notes          |
|----------------------------|------------------|-----|------------------|-------|----------------|
| Storage Temperature        | Tstg             | -50 | 85               | °C    |                |
| Operating Case Temperature | Topr             | 0   | 70               | °C    |                |
| Relative Humidity          | RH               | 0   | 85               | %     | Non condensing |
| Power Supply Voltage       | V <sub>CC3</sub> | 0   | 3.6              | V     |                |
| Input Voltage              | ---              | GND | V <sub>CC3</sub> | V     |                |

### Recommended Operating Conditions

| Parameter                  | Symbol           | Min  | Typ | Max  | Units / Notes |
|----------------------------|------------------|------|-----|------|---------------|
| Power Supply Voltage       | V <sub>CC3</sub> | 3.13 | 3.3 | 3.47 | V             |
| Power Supply Current       | I <sub>CC3</sub> |      | 360 | 550  | mA            |
| Power Dissipation          | P <sub>D</sub>   |      |     | 2    | W             |
| Operating Case Temperature | Topr             | 0    |     | 70   | °C            |
| Data Rate                  |                  |      | 8.5 |      | Gb/s          |

### Transmitter Optical Specifications (Topr= 0 to 70°C, Vcc5=5V±5%, Vcc3 = 3.3V ±5%)

| Parameter                               | Symbol              | Min                 | Typ            | Max                 | Units | Notes        |
|-----------------------------------------|---------------------|---------------------|----------------|---------------------|-------|--------------|
| Average Launch Power                    | P <sub>O, Avg</sub> | 1                   |                | 5                   | dBm   | 1            |
| Optical Modulation Amplitude            | P <sub>O, OMA</sub> | -1                  |                |                     | dBm   | 1            |
| Output Center Wavelength                | λ <sub>C</sub>      | λ <sub>C</sub> -5.5 | λ <sub>C</sub> | λ <sub>C</sub> +7.5 | nm    | 2            |
| Output Spectrum Width                   | σ <sub>λ</sub>      |                     |                | 1                   | nm    | -20 dB width |
| Side Mode Suppression Ratio             | SMSR                | 30                  |                |                     | dB    |              |
| Relative Intensity Noise                | RIN                 |                     |                | -130                | dB/Hz |              |
| Average Launch Power of OFF Transmitter |                     |                     |                | -30                 | dBm   |              |

1. Output power is power coupled into a 9/125 μm single-mode fiber.
2. ITU-T G.694.2 CWDM wavelength from 1350 nm to 1410 nm, each step 20 nm.

### Receiver Optical Specifications (Topr= 0 to 70°C, Vcc5=5V±5%, Vcc3 = 3.3V ±5%)

| Parameter               | Symbol           | Min  | Typ | Max  | Units | Notes                   |
|-------------------------|------------------|------|-----|------|-------|-------------------------|
| Sensitivity             | Sen1             |      |     | -15  | dBm   | 3                       |
| Receiver Overload       | P <sub>MAX</sub> | 0.5  | --- |      | dBm   |                         |
| LOS -- Deasserted       | LOS <sub>D</sub> | ---  | --- | -20  | dBm   | Transition: low to high |
| LOS -- Asserted         | LOS <sub>A</sub> | -32  | --- | ---  | dBm   | Transition: high to low |
| Wavelength of Operation | λ <sub>C</sub>   | 1260 |     | 1620 | nm    |                         |

3. Average received power; BER < 10<sup>-12</sup> and PRBS 2<sup>7</sup>-1

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| Electrical Characteristics                               |                  |     |     |                 |                  |                          |
|----------------------------------------------------------|------------------|-----|-----|-----------------|------------------|--------------------------|
| Parameter                                                | Symbol           | Min | Typ | Max             | Units            | Notes                    |
| <b>High-Speed Signal (CML) Interface Specification</b>   |                  |     |     |                 |                  |                          |
| Input Data Rate                                          |                  |     | 8.5 |                 | Gb/s             |                          |
| TX Clock Tolerance                                       |                  |     |     | ±100            | ppm              | 1                        |
| Differential Input Impedance                             | R <sub>in</sub>  |     | 100 |                 | Ω                |                          |
| Differential Data Input Amplitude                        |                  | 120 |     | 820             | mV <sub>pp</sub> | 2, Internally AC coupled |
| Output Data Rate                                         |                  |     | 8.5 |                 | Gb/s             |                          |
| RX Clock Tolerance                                       |                  |     |     | ±100            | ppm              | 1                        |
| Differential Output Impedance                            | R <sub>out</sub> |     | 100 |                 | Ω                |                          |
| Differential Data Output Amplitude                       |                  | 340 |     | 850             | mV <sub>pp</sub> | 2, Internally AC coupled |
| <b>Low-Speed Signal (LVTTTL) Interface Specification</b> |                  |     |     |                 |                  |                          |
| Input High Voltage                                       |                  | 2.0 |     | V <sub>cc</sub> | V                |                          |
| Input Low Voltage                                        |                  | GND |     | 0.8             | V                |                          |
| Output High Voltage                                      |                  | 2.4 |     | V <sub>cc</sub> | V                |                          |
| Output Low Voltage                                       |                  | GND |     | 0.5             | V                |                          |
| <b>Reference Clock (LVPECL) Interface Specification</b>  |                  |     |     |                 |                  |                          |
| No reference clock                                       |                  |     |     |                 |                  |                          |

1. Clock tolerance for 8.5Gb/s, 4.25Gb/s, 1.063Gb/s and 1.25Gb/s
2. The differential input and output amplitudes are per XFP MSA mask at points B' and C'.

| Transceiver Timing Characteristics |                           |     |     |     |       |       |
|------------------------------------|---------------------------|-----|-----|-----|-------|-------|
| Parameter                          | Symbol                    | Min | Typ | Max | Units | Notes |
| TX_DIS Assert Time                 | t <sub>off</sub>          |     |     | 10  | s     |       |
| TX_DIS Negate Time                 | t <sub>on</sub>           |     |     | 2   | ms    |       |
| Time to Initialize                 | t <sub>init</sub>         |     |     | 300 | ms    |       |
| Interrupt Assert Delay             | interrupt <sub>on</sub>   |     |     | 200 | ms    |       |
| Interrupt Negate Delay             | interrupt <sub>off</sub>  |     |     | 500 | s     |       |
| P_Down/PST Assert Delay            | P_Down/RST <sub>on</sub>  |     |     | 100 | s     |       |
| P_Down Negate Delay                | P_Down/RST <sub>off</sub> |     |     | 300 | ms    |       |
| Mod_NR Assert Delay                | Mod_nr <sub>on</sub>      |     |     | 1   | ms    |       |
| Mod_NR Negate Delay                | Mod_nr <sub>off</sub>     |     |     | 1   | ms    |       |
| Mod_Desel Assert Time              | T_Mod_Desel               |     |     | 2   | ms    |       |
| Mod_Desel De-Assert Time           | T_Mod_Sel                 |     |     | 2   | ms    |       |
| P_Down Reset Time                  | T <sub>reset</sub>        | 10  |     |     | s     |       |
| RX_LOS Assert Delay                | T_Los <sub>on</sub>       |     |     | 100 | s     |       |
| RX_LOS Negate Delay                | T_Los <sub>off</sub>      |     |     | 100 | s     |       |
| Serial ID Clock Rate               | f <sub>SCL</sub>          | 0   |     | 400 | kHz   |       |

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### MANAGEMENT INTERFACE

The structure of the memory map is shown in Figure 1, which is accessible over a 2-wire serial interface at the 8-bit address 1010000X (A0h). The normal 256 byte I2C address space is divided into low and upper blocks of 128 Bytes. The lower block of 128 Bytes is always directly available and is used for the diagnostics and control function. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. Thus, there is a total available address space of 128\*256 = 32 Kbytes in this upper memory space. The contents of Table 01h are listed in Table 1 below. Please refer SFF INF-8077i (Revision 4.5) for detailed information.



Figure 1. 2-wire Serial Digital Diagnostic Memory Map

Table 1 Monitoring Specification

| Data Address | Parameter   | Accuracy |
|--------------|-------------|----------|
| 96 ~ 97      | Temperature | ± 3°C    |
| 98 ~ 99      | Reserved    |          |
| 100 ~ 101    | Tx Bias     | ± 10%    |
| 102 ~ 103    | Tx Power    | ± 2dB    |
| 104 ~ 105    | Rx Power    | ± 2dB    |
| 106 ~ 107    | Vcc3        | ± 3%     |

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### CONNECTION DIAGRAM

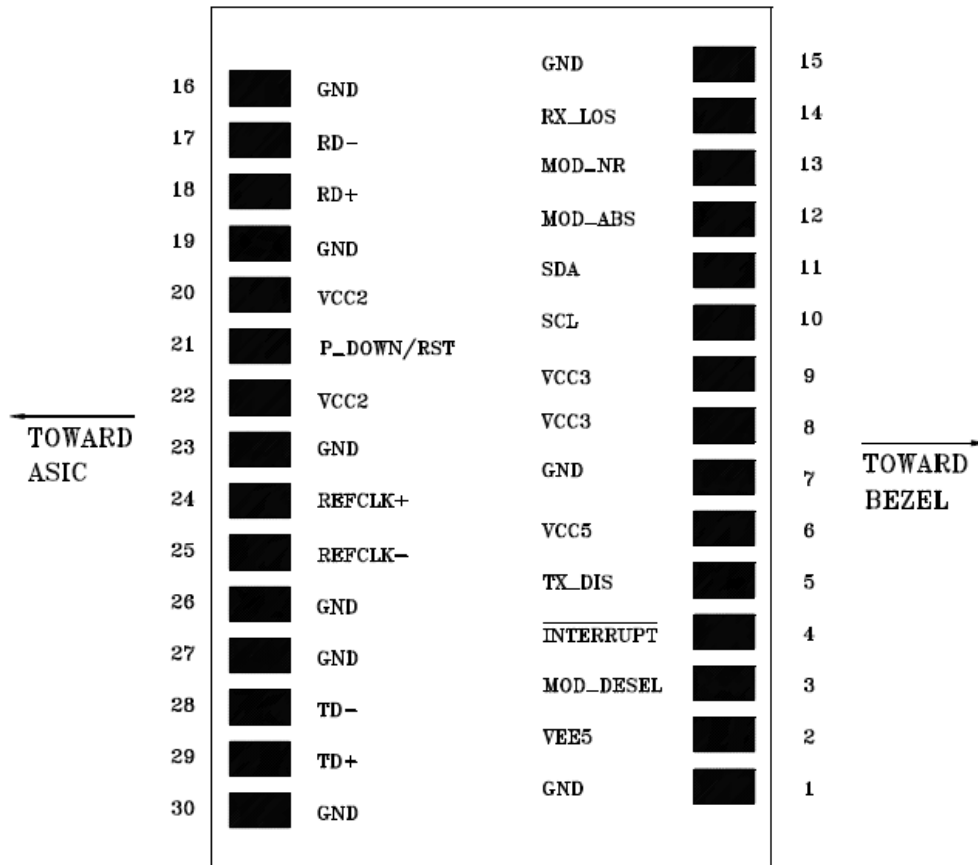


Table 3 PIN Description

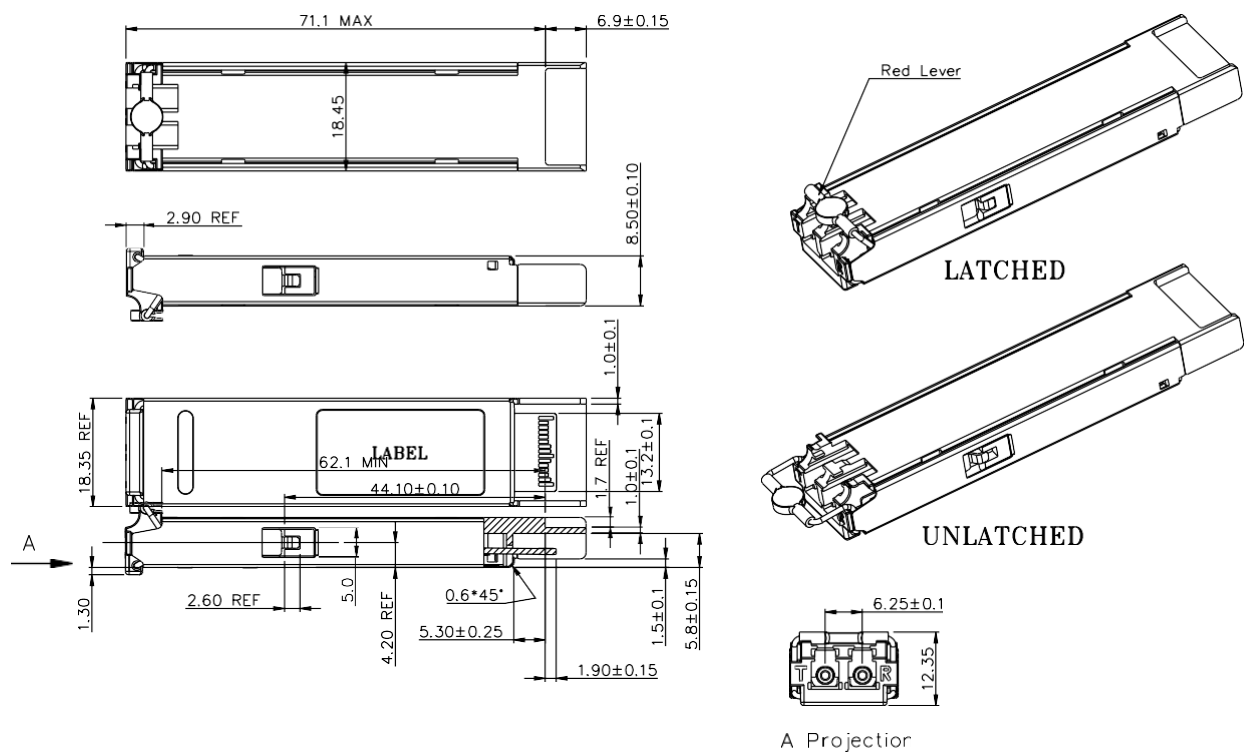
| PIN | Logic     | Signal Name | Description                                                                                                | Note |
|-----|-----------|-------------|------------------------------------------------------------------------------------------------------------|------|
| 1   |           | GND         | Module Ground                                                                                              | 1    |
| 2   |           | VEE5        | -5.2V Power Supply <b>(Not required)</b>                                                                   | 3    |
| 3   | LVTTL-I   | Mod_Desel   | Module De-select; When held low allows module to respond to 2-wire serial interface                        |      |
| 4   | LVTTL-O   | Interrupt   | Interrupt; Indicates presence of an important condition which can be read over the 2-wire serial interface | 2    |
| 5   | LVTTL-I   | TX_DIS      | Transmitter Disable; Turns off transmitter laser output                                                    |      |
| 6   |           | VCC5        | +5V Power Supply                                                                                           | 3    |
| 7   |           | GND         | Module Ground                                                                                              | 1    |
| 8   |           | VCC3        | +3.3V Power Supply                                                                                         |      |
| 9   |           | VCC3        | +3.3V Power Supply                                                                                         |      |
| 10  | LVTTL-I/O | SCL         | Serial 2-wire interface clock                                                                              | 2    |
| 11  | LVTTL-I/O | SDA         | Serial 2-wire interface data line                                                                          | 2    |
| 12  | LVTTL-O   | Mod_Abs     | Indicates Module is not present. Grounded in the Module                                                    | 2    |
| 13  | LVTTL-O   | Mod_NR      | Module Not Ready; Indicating Module Operational Fault                                                      | 2    |
| 14  | LVTTL-O   | RX_LOS      | Receiver Loss Of Signal Indicator                                                                          | 2    |
| 15  |           | GND         | Module Ground                                                                                              | 1    |
| 16  |           | GND         | Module Ground                                                                                              | 1    |
| 17  | CML-O     | RD-         | Receiver Inverted Data Output                                                                              |      |
| 18  | CML-O     | RD+         | Receiver Non-Inverted Data Output                                                                          |      |
| 19  |           | GND         | Module Ground                                                                                              | 1    |
| 20  |           | VCC2        | +1.8V Power Supply <b>(Not required)</b>                                                                   | 3    |

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|    |          |            |                                                                                                                                                                                                                                                                                                   |   |
|----|----------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|
| 21 | LVTTTL-I | P_Down/RST | Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode.<br>Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle. |   |
| 22 |          | VCC2       | +1.8V Power Supply ( <b>Not required</b> )                                                                                                                                                                                                                                                        | 3 |
| 23 |          | GND        | Module Ground                                                                                                                                                                                                                                                                                     | 1 |
| 24 | PECL-I   | RefCLK+    | Reference Clock Non-Inverted Input, AC coupled on the host board. ( <b>Not used. Internally terminated to 50 ohm (100 ohm diff.)</b> )                                                                                                                                                            | 4 |
| 25 | PECL-I   | RefCLK-    | Reference Clock Inverted Input, AC coupled on the host board. ( <b>Not used. Internally terminated to 50 ohm (100 ohm diff.)</b> )                                                                                                                                                                | 4 |
| 26 |          | GND        | Module Ground                                                                                                                                                                                                                                                                                     | 1 |
| 27 |          | GND        | Module Ground                                                                                                                                                                                                                                                                                     | 1 |
| 28 | CML-I    | TD-        | Transmitter Inverted Data Input                                                                                                                                                                                                                                                                   |   |
| 29 | CML-I    | TD+        | Transmitter Non-Inverted Data Input                                                                                                                                                                                                                                                               |   |
| 30 |          | GND        | Module Ground                                                                                                                                                                                                                                                                                     | 1 |

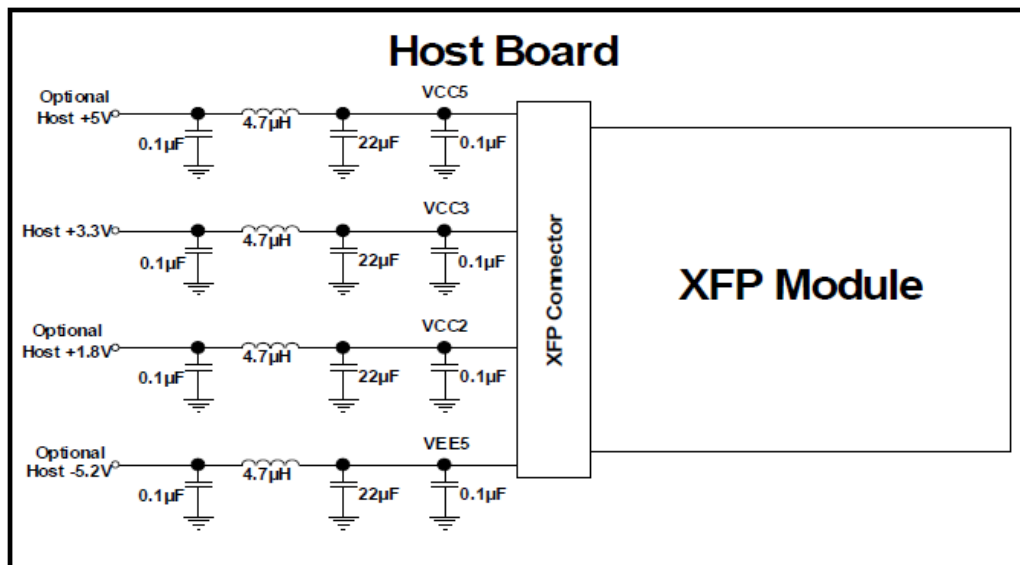
1. Module ground pins GND are isolated from the module case and chassis ground within the module.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.
3. These PINs are open within module.
4. A Reference Clock input is not required. If present, it will be ignored.

## MECHANICAL SPECIFICATION (UNITS IN MM)



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### RECOMMENDED POWER CIRCUIT SCHEMATIC



### RECOMMENDED INTERFACE CIRCUIT

