

Professional high-speed optical transceiver

OPN-XS13-40LC2 / OPN-XS13-40LC2I

8.5Gb/s 1310 nm XFP Single-Mode Optical Transceiver for 8G FC Applications

PRODUCT FEATURES

- Up to 8.5 Gb/s Bi-directional Data Link
 - Complaint with XFP MSA
- Compliant with Fiber Channel FC-PI-4 800-SN-LL-I
 - Compliant with 4G, 2G Fiber Channel
 - 1310 nm DFB LD Transmitter
 - AC/AC Coupling according to MSA
 - Distance up to 40 km
- 2-Wire Interface for Integrated Digital Diagnostic Monitoring
 - XFI Loopback Mode
 - No reference Clock required
 - Power Consumption < 2 W
- Only Required +3.3 V Power Supply
 - RoHS Compliant
- 0 to 70°C Operating : OPN-XS13-40LC2
- -50 to 85°C Operating : OPN-XS13-40LC2I
 - Duplex LC Connector

APPLICATIONS

- Multi-rate 8x/4x/2x Fibre Channel

STANDARD

- Compliant with XFP MSA
- Compliant with 8GFC

PRODUCT DESCRIPTION

OPN-XS13-40LC2 series multi-rate 8G XFP transceivers are designed for serial optical data communications such as 8G Fibre Channel. It supports the 8.5Gbps transmission on 9/125 µm SMF.

The transceiver consists of two sections: The transmitter section consists of a directly modulated 1310 nm multiple quantum well DFB laser, driver and signal conditioner. The receiver section incorporates a PIN photodiode integrated with a trans-impedance preamplifier (TIA) and signal conditioner.

The module is with the XFP 30-pin connector to allow hot plug capability. Integrated Tx and Rx signal conditioners provide high jitter-tolerance for full XFI compliance and no external reference clock required. The internally ac coupled high speed serial I/O simplifies interfacing to external circuitry. Only single 3.3V power supply is needed. The optical output can be disabled by LVTTTL logic high-level input of TX_DIS. Loss of signal (RX_LOS) output is provided to indicate the loss of an input optical signal of receiver.

A serial EEPROM in the transceiver allows the user to access transceiver digital diagnostic monitoring and configuration data via the 2-wire XFP Management Interface. This interface uses a single address, A0h, with a memory map divided into a lower and upper area. Basic digital diagnostic data is held in the lower area while specific data is held in a series of tables in the high memory area.

ORDER INFORMATION

P/No.	Bit Rate (Gb/s)	Distance (km)	Wavelength (nm)	Package	Connector	Case Temp (°C)	RoHS Compliant
OPN-XS13-40LC2	8 / 4 / 2	40	1310 DFB	XFP with DMI	LC	0 to 70	Yes
OPN-XS13-40LC2I	8 / 4 / 2	40	1310 DFB	XFP with DMI	LC	-50 to 85	Yes

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Absolute Maximum Ratings					
Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	Tstg	-50	85	°C	
Operating Case Temperature	Topr	0 -50	70 85	°C	OPN-XS13-40LC2 OPN-XS13-40LC2I
Relative Humidity	RH	0	85	%	Non condensing
Power Supply Voltage	V _{CC3}	0	3.6	V	
Input Voltage	---	GND	V _{CC3}	V	

Recommended Operating Conditions					
Parameter	Symbol	Min	Typ	Max	Units / Notes
Power Supply Voltage	V _{CC3}	3.13	3.3	3.47	V
Power Supply Current (@3.3V)	I _{CC3}		360	550	mA
Power Dissipation	P _D			2	W
Operating Case Temperature	Topr	0 -50		70 85	°C / OPN-XS13-40LC2 °C / OPN-XS13-40LC2I
Data Rate			8.5		Gb/s

Transmitter Optical Specifications (Topr= 0 to 70°C, Vcc3 = 3.3V ±5%)					
Parameter	Symbol	Min	Typ	Max	Units / Notes
Average Launch Power	P _{O, Avg}	1		4	dBm / 1
Output Center Wavelength	λ _c	1260	1310	1360	nm
Output Spectrum Width	σ _λ			1	nm / -20 dB width
Side Mode Suppression Ratio	SMSR	30			dB
Relative Intensity Noise	RIN			-130	dB/Hz
Average Launch Power of OFF Transmitter				-30	dBm

1. Output power is power coupled into a 9/125 μm single-mode fiber.

Receiver Optical Specifications (Topr= 0 to 70°C, Vcc3 = 3.3V ±5%)					
Parameter	Symbol	Min	Typ	Max	Units / Notes
Sensitivity at 8.5 Gb/s	Sens			-15	dBm / 2
Receiver Overload	P _{MAX}	0.5	---		dBm
LOS -- Deasserted	LOS _D	---	---	-20	dBm / Transition: low to high
LOS -- Asserted	LOS _A	-30	---	---	dBm / Transition: high to low
Wavelength of Operation	λ _c	1260		1580	nm

2. Measured with worst ER; BER < 10⁻¹² and PRBS 2⁷-1.

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Electrical Characteristics						
Parameter	Symbol	Min	Typ	Max	Units	Notes
High-Speed Signal (CML) Interface Specification						
Input Data Rate			8.5		Gb/s	
TX Clock Tolerance				±100	ppm	1
Differential Input Impedance	R _{in}		100		Ω	
Differential Data Input Amplitude		120		820	mV _{pp}	2, Internally AC coupled
Output Data Rate			8.5		Gb/s	
RX Clock Tolerance				±100	ppm	1
Differential Output Impedance	R _{out}		100		Ω	
Differential Data Output Amplitude		340		850	mV _{pp}	2, Internally AC coupled
Low-Speed Signal (LVTTTL) Interface Specification						
Input High Voltage		2.0		V _{cc}	V	
Input Low Voltage		GND		0.8	V	
Output High Voltage		2.4		V _{cc}	V	
Output Low Voltage		GND		0.5	V	
Reference Clock (LVPECL) Interface Specification						
No reference clock						

1. Clock tolerance for 8.5Gb/s, 4.25Gb/s, 1.063Gb/s and 1.25Gb/s
2. The differential input and output amplitudes are per XFP MSA mask at points B' and C'.

Transceiver Timing Characteristics						
Parameter	Symbol	Min	Typ	Max	Units	Notes
TX_DIS Assert Time	t _{off}			10	μs	
TX_DIS Negate Time	t _{on}			2	ms	
Time to Initialize	t _{init}			300	ms	
Interrupt Assert Delay	interrupt _{on}			200	ms	
Interrupt Negate Delay	interrupt _{off}			500	μs	
P_Down/PST Assert Delay	P_Down/RST _{on}			100	μs	
P_Down Negate Delay	P_Down/RST _{off}			300	ms	
Mod_NR Assert Delay	Mod_nr _{on}			1	ms	
Mod_NR Negate Delay	Mod_nr _{off}			1	ms	
Mod_Desel Assert Time	T_Mod_Desel			2	ms	
Mod_Desel De-Assert Time	T_Mod_Sel			2	ms	
P_Down Reset Time	T _{reset}	10			μs	
RX_LOS Assert Delay	T_Los _{on}			100	μs	
RX_LOS Negate Delay	T_Los _{off}			100	μs	
Serial ID Clock Rate	f _{SCL}	0		400	kHz	

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Management Interface

The structure of the memory map is shown in Figure 1, which is accessible over a 2-wire serial interface at the 8-bit address 1010000X (A0h). The normal 256 byte I2C address space is divided into low and upper blocks of 128 Bytes. The lower block of 128 Bytes is always directly available and is used for the diagnostics and control function. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. Thus, there is a total available address space of $128 \times 256 = 32$ Kbytes in this upper memory space. The contents of Table 01h are listed in Table 1 below. Please refer SFF INF-8077i (Revision 4.5) for detailed information.

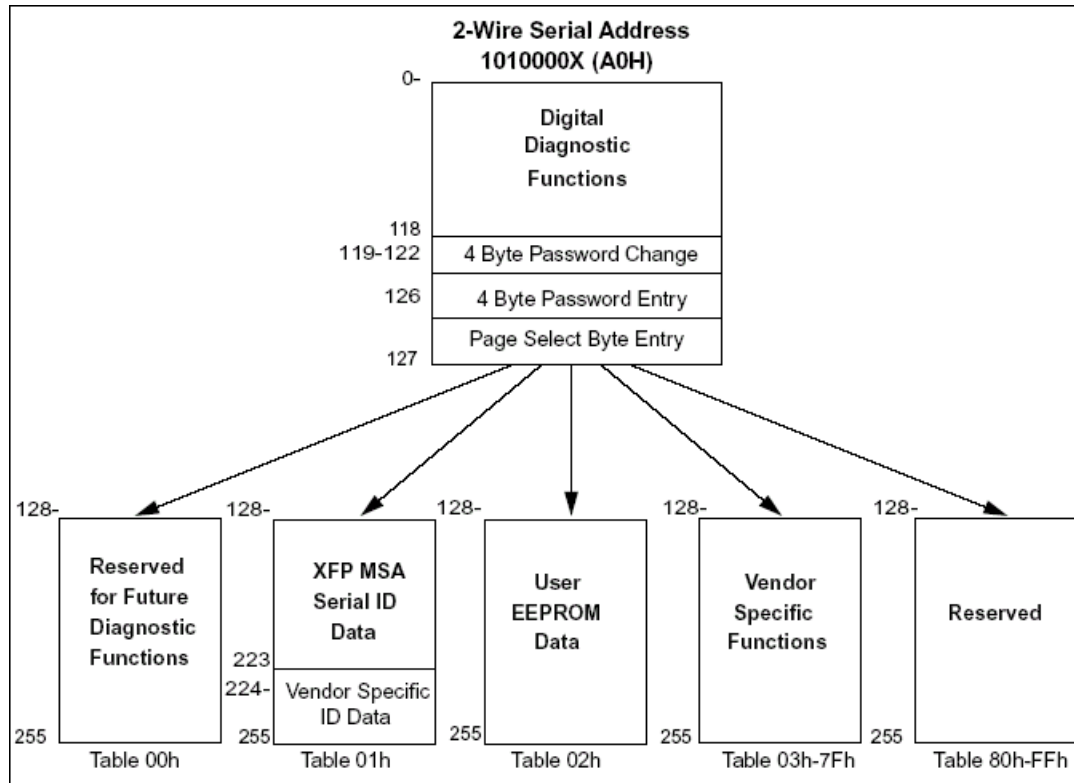


Figure 1. 2-wire Serial Digital Diagnostic Memory Map

Table 1 Monitoring Specification

Data Address	Parameter	Accuracy
96 ~ 97	Temperature	± 3°C
98 ~ 99	Reserved	
100 ~ 101	Tx Bias	± 10%
102 ~ 103	Tx Power	± 2dB
104 ~ 105	Rx Power	± 2dB
106 ~ 107	Vcc3	± 3%

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CONNECTION DIAGRAM

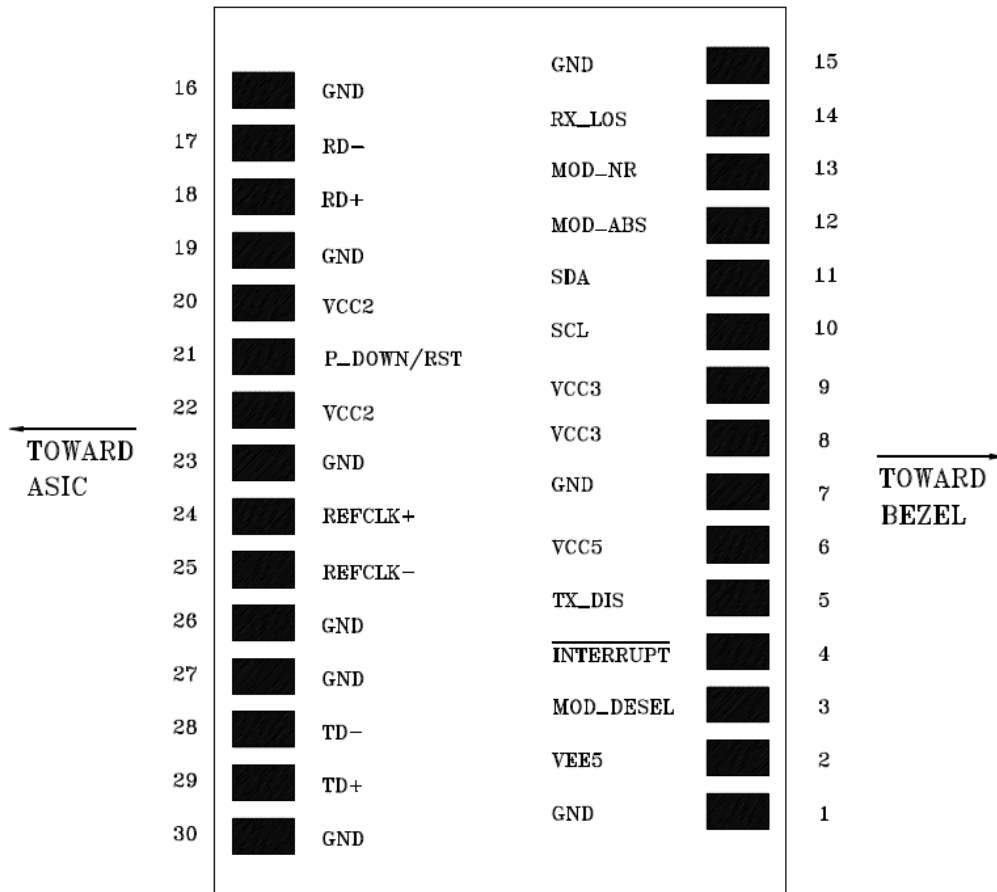


Table 3 PIN Description

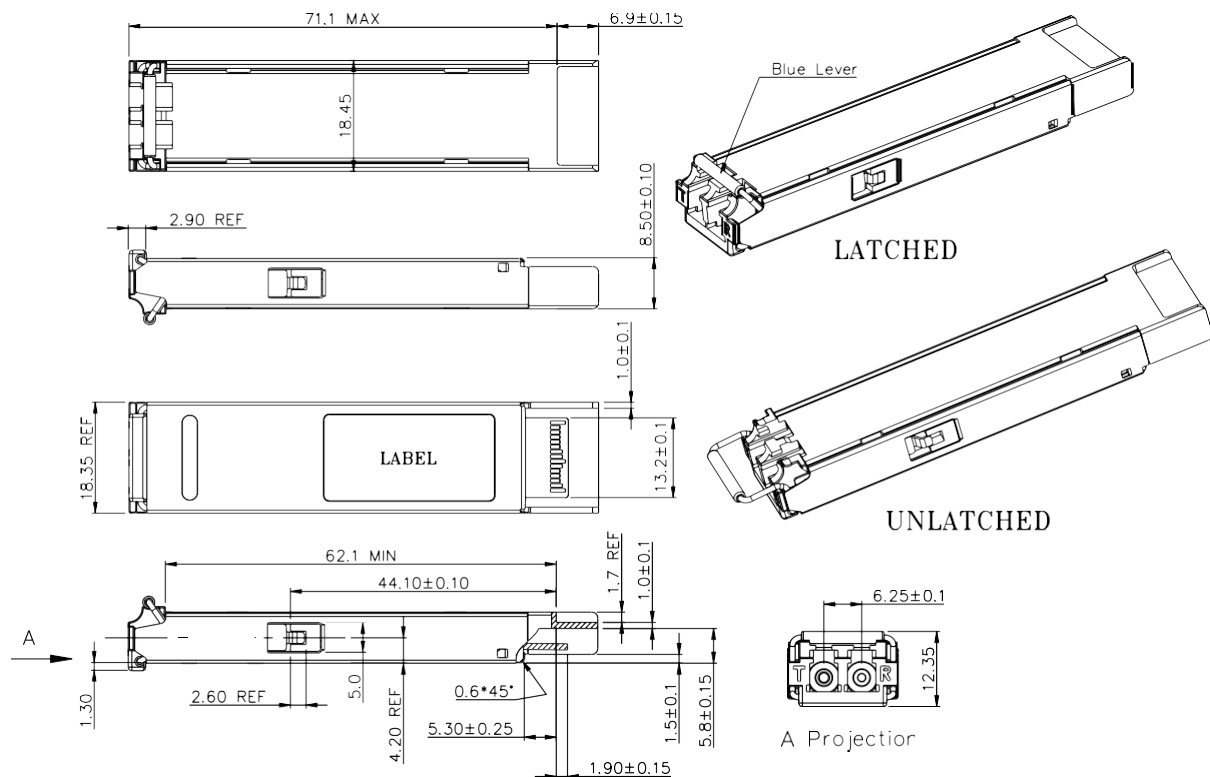
PIN	Logic	Signal Name	Description	Note
1		GND	Module Ground	1
2		VEE5	-5.2V Power Supply (Not required)	3
3	LVTTL-I	Mod_Desel	Module De-select; When held low allows module to respond to 2-wire serial interface	
4	LVTTL-O	Interrupt	Interrupt; Indicates presence of an important condition which can be read over the 2wire serial interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Turns off transmitter laser output	
6		VCC5	+5V Power Supply (Not required)	3
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I/O	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Indicates Module is not present. Grounded in the Module	2
13	LVTTL-O	Mod_NR	Module Not Ready; Indicating Module Operational Fault	2
14	LVTTL-O	RX_LOS	Receiver Loss Of Signal Indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver Inverted Data Output	
18	CML-O	RD+	Receiver Non-Inverted Data Output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply (Not required)	3

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21	LVTTTL-I	P_Down/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode. Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply (Not required)	3
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock Non-Inverted Input, AC coupled on the host board. (Not used. Internally terminated to 50 ohm (100 ohm diff.))	4
25	PECL-I	RefCLK-	Reference Clock Inverted Input, AC coupled on the host board. (Not used. Internally terminated to 50 ohm (100 ohm diff.))	4
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter Inverted Data Input	
29	CML-I	TD+	Transmitter Non-Inverted Data Input	
30		GND	Module Ground	1

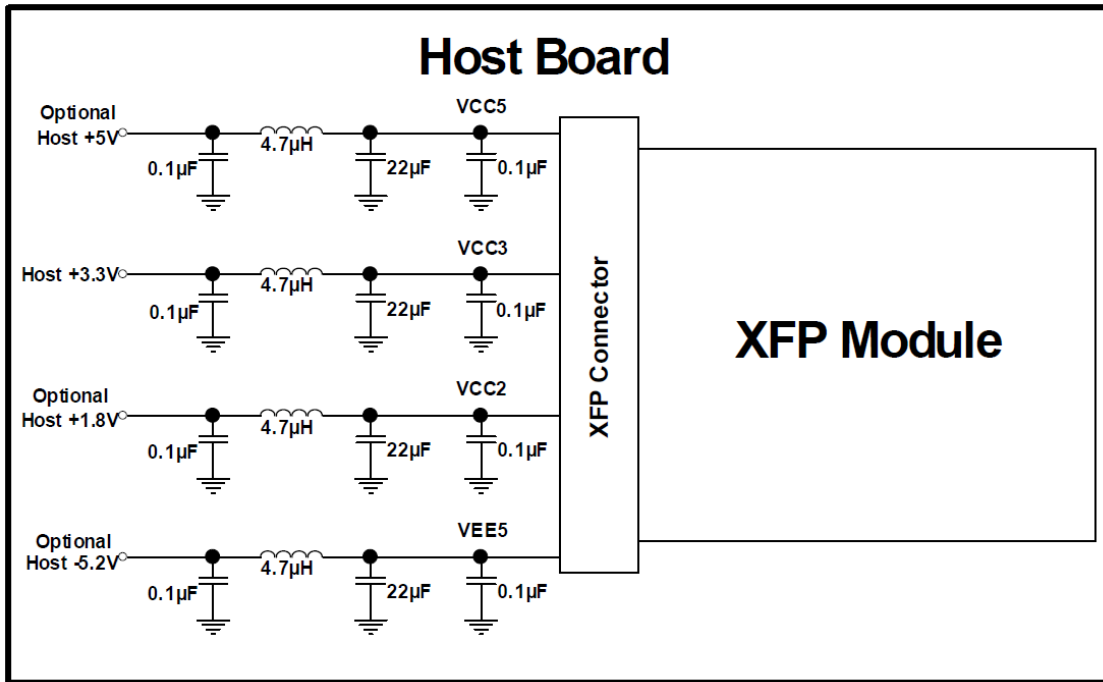
1. Module ground pins GND are isolated from the module case and chassis ground within the module.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.
3. These PINs are open within module.
4. A Reference Clock input is not required. If present, it will be ignored.

MECHANICAL SPECIFICATION (UNITS IN MM)



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RECOMMENDED POWER CIRCUIT SCHEMATIC



RECOMMENDED INTERFACE CIRCUIT

