Professional high-speed optical transceiver

OPN-XHD41-40LC2

10Gbps / 40 km / 100GHz DWDM XFP Single-Mode Optical Transceiver for 10GbE / OC-412

PRODUCT FEATURES

- Support 9.95 Gbps to 10.5 Gbps
- Complaint with XFP MSA
- Compliant with XFI 10G Serial Electrical Interface
- Maximum Link Length of 40 km
- Temperature-stabilized DWDM EML Transmitter
- 100 GHz ITU Grid, C Band
- 2-Wire Interface for Integrated Digital DiagnosticMonitoring
- XFI Loopback Mode Supported
- No reference Clock required
- Power Dissipation < 3.5 W
- Dual 5V and +3.3 V Power Supply
- RoHS Compliant
- 0 to 70ºC Case Operating Temperature

APPLICATIONS

- 10GBASE-ER at 10.3125 Gb/s
- 10GBASE-EW at 9.953 Gb/s
- 40km 10GFC at 10.51875 Gb/s
- 10G SONET/SDH

PRODUCT DESCRIPTION

OPN-XHD41-40LC2 series DWDM transceivers are designed for single-mode fibre serial optical data communications such as 10G Ethernet 10GBASE-ER/EWand 10G Fibre Channel.

This module is designed for single mode fiber andoperates at a nominal wavelength of 100GHz ITU Grid, C Band DWDM wavelength. A guaranteed minimum opticallink budget of 14 dB is offered. The transmitter section consists of a temperature-stabilized DWDM electrical-modulated laser (EML), driver and signal conditioner. The receiver section incorporates a PIN photodiode integrated with a trans-impedance preamplifier(TIA) and signal conditioner.

The module is with the XFP 30-pin connector to allow hot plug capability. Integrated Tx and Rx signal conditioners provide high jitter-tolerance for full XFI compliance and noexternal reference clock required. The internally ac coupledhigh speed serial I/O simplifies interfacing to externalcircuitry. Dual 5V and 3.3V power supply are used. The optical output can be disabled by LVTTL logic high-level input of TX_DIS. Loss of signal (RX_LOS) output isprovided to indicate the loss of an input optical signal of receiver.

A serial EEPROM in the transceiver allows the user to access transceiver digital diagnostic monitoring and configuration data via the 2-wire XFP Management Interface. This interface uses a single address, A0h, with amemory map divided into a lower and upper area. Basic digital diagnostic data is held in the lower area while specificdata is held in a series of tables in the high memory area.

ORDER INFORMATION

P/No.	Bit Rate(Gb/s)	10G	Distance (km)	Spacing (GHz)	Wavelength (nm)	Package	Case Temp (ºC)	RoHS Compliant
OPN-XHD41-40LC2	9.95-10.52	ER/EW	40	100	DWDM*	XFP with DMI	0 to 70	Yes

XX: 100GHz ITU Grid wavelength (Please see below)

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Channel #	Product code	Frequency (THz)	Center Wavelength (nm)	Label
19	OPN-XHD19-40LC2	191.9	1562.23	D19
20	OPN-XHD20-40LC2	192.0	1561.42	D20
21	OPN-XHD21-40LC2	192.1	1560.61	D21
22	OPN-XHD22-40LC2	192.2	1559.79	D22
23	OPN-XHD23-40LC2	192.3	1558.98	D23
24	OPN-XHD24-40LC2	192.4	1558.17	D24
25	OPN-XHD25-40LC2	192.5	1557.36	D25
26	OPN-XHD26-40LC2	192.6	1556.55	D26
27	OPN-XHD27-40LC2	192.7	1555.75	D27
28	OPN-XHD28-40LC2	192.8	1554.94	D28
29	OPN-XHD29-40LC2	192.9	1554.13	D29
30	OPN-XHD30-40LC2	193.0	1553.33	D30
31	OPN-XHD31-40LC2	193.1	1552.52	D31
32	OPN-XHD32-40LC2	193.2	1551.72	D32
33	OPN-XHD33-40LC2	193.3	1550.92	D33
34	OPN-XHD34-40LC2	193.4	1550.12	D34
35	OPN-XHD35-40LC2	193.5	1549.32	D35
36	OPN-XHD36-40LC2	193.6	1548.51	D36
37	OPN-XHD37-40LC2	193.7	1547.72	D37
38	OPN-XHD38-40LC2	193.8	1546.92	D38
39	OPN-XHD39-40LC2	193.9	1546.12	D39
40	OPN-XHD40-40LC2	194.0	1545.32	D40
41	OPN-XHD41-40LC2	194.1	1544.53	D41
42	OPN-XHD42-40LC2	194.2	1543.73	D42
43	OPN-XHD43-40LC2	194.3	1542.94	D43
44	OPN-XHD44-40LC2	194.4	1542.14	D44
45	OPN-XHD45-40LC2	194.5	1541.35	D45
46	OPN-XHD46-40LC2	194.6	1540.56	D46
47	OPN-XHD47-40LC2	194.7	1539.77	D47
48	OPN-XHD48-40LC2	194.8	1538.98	D48
49	OPN-XHD49-40LC2	194.9	1538.19	D49
50	OPN-XHD50-40LC2	195.0	1537.40	D50
51	OPN-XHD51-40LC2	195.1	1536.61	D51
52	OPN-XHD52-40LC2	195.2	1535.82	D52
53	OPN-XHD53-40LC2	195.3	1535.04	D53
54	OPN-XHD54-40LC2	195.4	1534.25	D54
55	OPN-XHD55-40LC2	195.5	1533.47	D55
56	OPN-XHD56-40LC2	195.6	1532.68	D56
57	OPN-XHD57-40LC2	195.7	1531.90	D57
58	OPN-XHD58-40LC2	195.8	1531.12	D58
59	OPN-XHD59-40LC2	195.9	1530.33	D59
60	OPN-XHD60-40LC2	196.0	1529.55	D60
61	OPN-XHD61-40LC2	196.1	1528.77	D61

Absolute Maximum Ratings					
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Notes**
Storage Temperature	Tstg	-50	85	^{o}C	
Operating Case Temperature	Topr	0	70	^{o}C	
Relative Humidity	RH	0	85	%	Non condensing
Power Supply Voltage (5V)	Vcc5	-0.5	3.6	V	
Power Supply Voltage (3.3V)	$V_{CC}3$	-0.5	3.6	V	
Receiver Input Optical Power	Mip		4	dBm	Received average power

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Recommended Operating Conditions					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units / Notes**
Power Supply Voltage (5V)	$V_{CC}5$	4.75	5	5.25	V
Power Supply Voltage (3.3V)	$V_{CC}3$	3.13	3.3	3.47	V
Power Supply Current (@5V)	$I_{CC}5$			300	mA / 1
Power Supply Current (@3.3V)	$I_{CC}3$			750	mA / 1
Power Dissipation	P_D			3.5	W
Operating Case Temperature	Topr	0		70	ºC
Data Rate		9.95	10.3125	10.5	Gb/s

1. Including in rush current. Maximum module current ramp rate is 100 mA/µs.

Transmitter Optical Specifications (Topr= 0 to 70ºC, Vcc5=5V±5%, Vcc3 = 3.3V ±5%)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Average Launch Power	$P_{o,\ Avg}$	-2		+2	dBm	2
Extinction Ratio	ER	8.2			dB	
Center Wavelength Spacing			100		GHz	3
Transmitter Center Wavelength -- over life time	λc	X-100	X	X+100	pm	4
Output Spectrum Width	σ_λ			1	nm	-20 dB width
Side Mode Suppression Ratio	SMSR	30			dB	
Transmitter and Dispersion Penalty @ 800 ps/nm	TDP			2	dB	
Relative Intensity Noise	RIN			-130	dB/Hz	10G Ethernet
Eye Mask	1EEE 802.3ae					
Average Launch Power of OFF Transmitter				-30	dBm	

2. Output power is power coupled into a 9/125 µm single-mode fiber.
3. Corresponds to approximately 0.8 nm.
4. X = specified ITU Grid wavelength. Wavelength stability is achieved within 60 seconds of power up.

Receiver Optical Specifications (Topr= 0 to 70ºC, Vcc5=5V±5%,Vcc3 = 3.3V ±5%)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Sensitivity	Sen1			-16	dBm	5
Stressed Receiver Sensitivity, OMA	Sen2			-11.3	dBm	
Receiver Overload	P_{MAX}	-1	---		dBm	
LOS -- Deasserted	LOS_D	---	---	-20	dBm	Transition: low to high
LOS -- Asserted	LOS_A	-28	---	---	dBm	Transition: high to low
LOS -- Hysteresis		0.5	---		dB	
Wavelength of Operation	λc	1260		1600	nm	
Optical Return Loss	ORL			-27	dB	

5. Measured with worst ER; BER < 10^{-12} and PRBS 2^{31}-1. Equivalent to -14.3 dBm OMA at ER=8.2 dB.

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Electrical Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
High-Speed Signal (CML) Interface Specification						
Input Data Rate		9.95	10.3125	10.5	Gb/s	6
Differential Input Impedance	Rin		100		Ω	
Differential Data Input Amplitude		120		820	mVpp	7, Internally AC coupled
Output Data Rate		9.95	10.3125	10.5	Gb/s	6
Differential Output Impedance	Rout		100		Ω	
Differential Data Output Amplitude		340	650	850	mVpp	7, Internally AC coupled
Low-Speed Signal (LVTTL) Interface Specification						
Input High Voltage		2.0		Vcc	V	
Input Low Voltage		GND		0.8	V	
Output High Voltage		2.4		Vcc	V	
Output Low Voltage		GND		0.5	V	
Reference Clock (LVPECL) Interface Specification						
No reference clock required.						

6. 10GBASE-ER/EW and 10G Fiber Channel.
7. The differential input and output amplitudes are per XFP MSA mask at points B' and C'.

Transceiver Timing Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
TX_DIS Assert Time	t_off			10	µs	
TX_DIS Negate Time	t_on			2	ms	
Time to Initialize	t_init			300	ms	
Interrupt Assert Delay	interrupt_on			200	ms	
Interrupt Negate Delay	interrupt_off			500	µs	
P_Down/PST Assert Delay	P_Down/RST_on			100	µs	
P_Down Nagate Delay	P_Down/RST_off			300	ms	
Mod_NR Assert Delay	Mod_nr_on			1	ms	
Mod_NR Negate Delay	Mod_nr_off			1	ms	
Mod_Desel Assert Time	T_Mod_Desel			2	ms	
Mod_Desel De-Assert Time	T_Mod_Sel			2	ms	
P_Down Reset Time	T_reset	10			µs	
RX_LOS Assert Delay	T_Los_on			100	µs	
RX_LOS Negate Delay	T_Los_off			100	µs	
Serial ID Clock Rate	f_{SCL}	0		400	kHz	

MANAGEMENT INTERFACE

The structure of the memory map is shown in Figure 1, which is accessible over a 2-wire serial interface at the 8-bit address 1010000X (A0h). The normal 256 byte I2C address space is divided into low and upper blocks of 128 Bytes. The lower block of 128 Bytes is always directly available and is used for the diagnostics and control function. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. Thus, there is a total available address space of 128*256 = 32 Kbytes in this upper memory space. The contents of Table 01h are listed in Table 1 below. Please refer SFF INF-8077i (Revision 4.5) for detailed information.

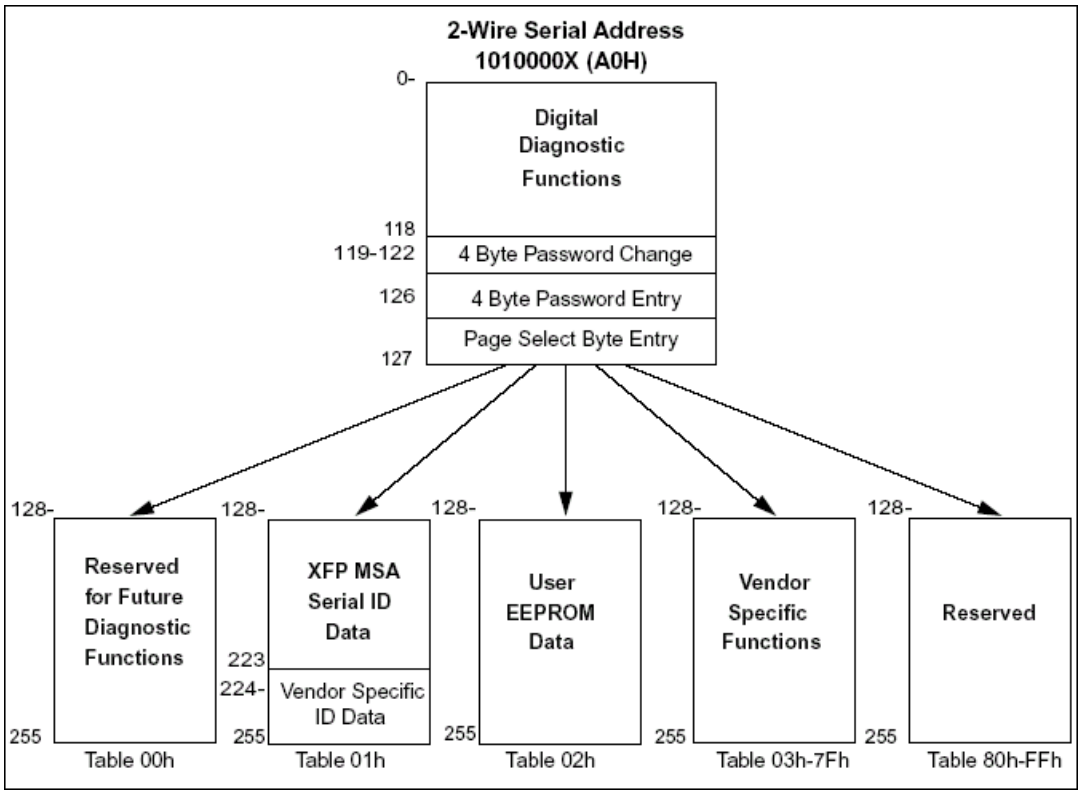

Figure 1. 2-wire Serial Digital Diagnostic Memory Map

Table 1 Monitoring Specification

Data Address	Parameter	Accuracy
96 ~ 97	Temperature	± 3ºC
98 ~ 99	Reserved	
100 ~ 101	Tx Bias	± 10%
102 ~ 103	Tx Power	± 2dB
104 ~ 105	Rx Power	± 2dB
106 ~ 107	Vcc3	± 3%

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CONNECTION DIAGRAM

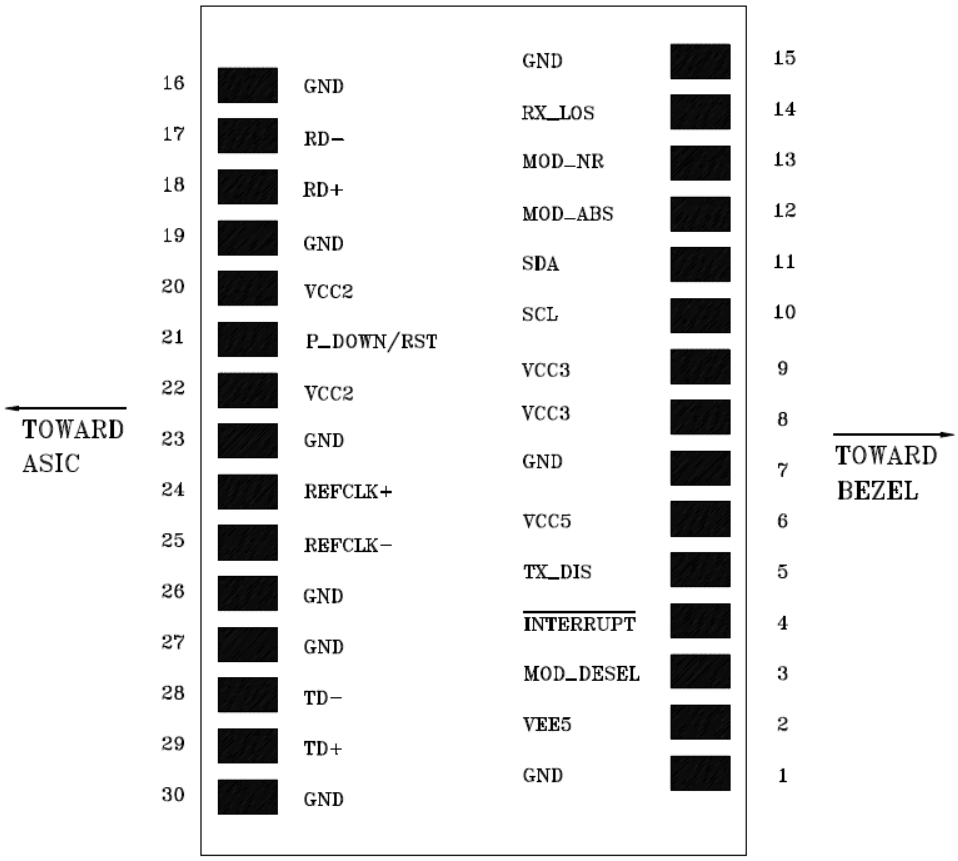

Table 2 PIN Description

PIN	Logic	Signal Name	Description	Note
1		GND	Module Ground	1
2		VEE5	-5.2V Power Supply **(Not required)**	3
3	LVTTL-I	Mod_Desel	Module De-select; When held low allows module to respond to 2-wire serial interface	
4	LVTTL-O	$\overline{\text{Interrupt}}$	Interrupt; Indicates presence of an important condition which can be read over the 2wire serial interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Turns off transmitter laser output	
6		VCC5	+5V Power Supply	3
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I/O	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Indicates Module is not present. Grounded in the Module	2
13	LVTTL-O	Mod_NR	Module Not Ready; Indicating Module Operational Fault	2
14	LVTTL-O	RX_LOS	Receiver Loss Of Signal Indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver Inverted Data Output	
18	CML-O	RD+	Receiver Non-Inverted Data Output	
41		GND	Module Ground	1
20		VCC2	+1.8V Power Supply **(Not required)**	3

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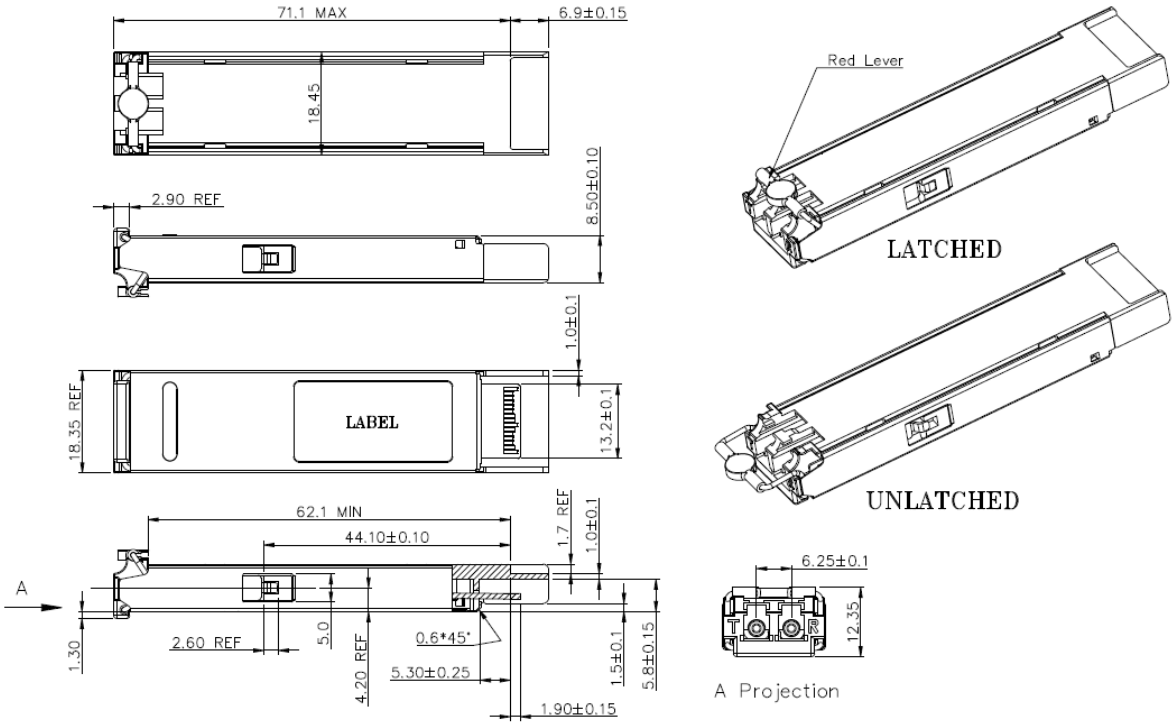
21	LVTTL-I	P_Down/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode.	
			Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply **(Not required)**	3
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock Non-Inverted Input, AC coupled on the host board. **(Not used. Internally terminated to 50 ohm (100 ohm diff.))**	4
25	PECL-I	RefCLK-	Reference Clock Inverted Input, AC coupled on the host board. **(Not used. Internally terminated to 50 ohm (100 ohm diff.))**	4
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter Inverted Data Input	
29	CML-I	TD+	Transmitter Non-Inverted Data Input	
30		GND	Module Ground	1

1. Module ground pins GND are isolated from the module case and chassis ground within the module.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.
3. These PINs are open within module.
4. A Reference Clock input is not required. If present, it will be ignored.

MECHANICAL SPECIFICATION (UNITS IN MM)



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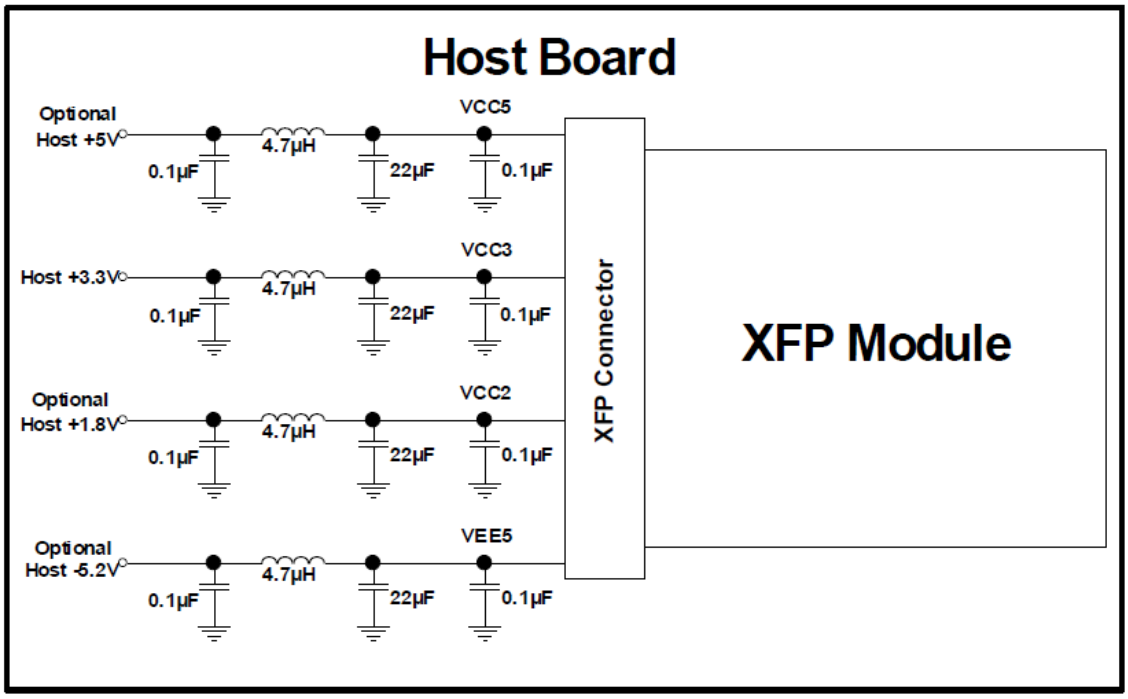
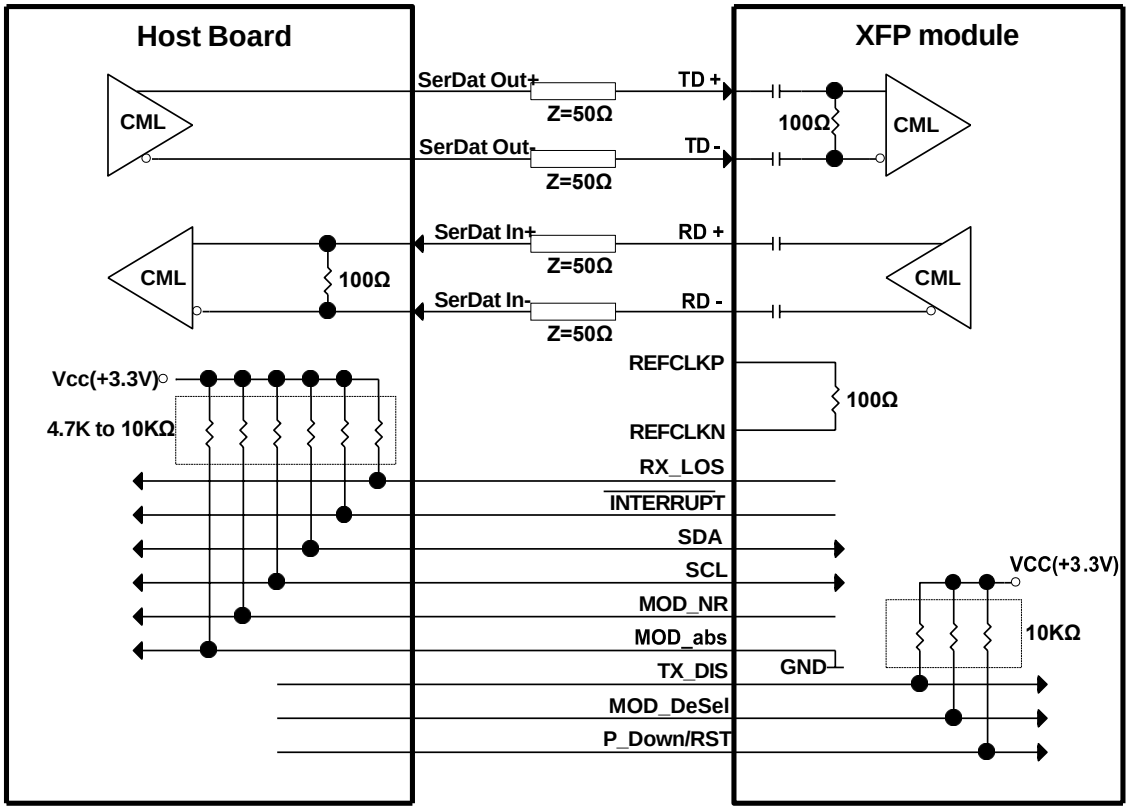
RECOMMENDED POWER CIRCUIT SCHEMATIC



RECOMMENDED INTERFACE CIRCUIT