

Professional high-speed optical transceiver

OPN-XH15-40LC2 / OPN-XH15-40LC2I

10Gbps / 40km / 1550 nm XFP Single-Mode Optical Transceiver for 10GbE / 10G FC

PRODUCT FEATURES

- Support 9.95 Gbps to 10.5 Gbps
 - Complaint with XFP MSA
- Compliant with XFI 10G Serial Electrical Interface
 - Maximum Link Length of 40 km
- Temperature-stabilized 1550 nm EML Transmitter
- 2-Wire Interface for Integrated Digital Diagnostic Monitoring
 - XFI Loopback Mode
 - No reference Clock required
 - Power Dissipation < 3.5 W
- Dual 5V and 3.3 V Power Supply
 - RoHS Compliant
- 0 to 70°C Operating: OPN-XH15-40LC2
- -50 to 85°C Operating: OPN-XH15-40LC2I

APPLICATIONS

- 10GBASE-ER/EW
- 40 km 10G Fibre Channel

PRODUCT DESCRIPTION

OPN-XH15-40LC2 series transceivers are designed for single-mode fibre serial optical data communications such as 10G Ethernet 10GBASE-ER/EW and 10G Fibre Channel.

The transceiver consists of two sections: The transmitter section consists of a temperature-stabilized 1550 nm electrical-modulated laser (EML), driver and signal conditioner. The receiver section incorporates a PIN photodiode integrated with a trans-impedance preamplifier (TIA) and signal conditioner.

The module is with the XFP 30-pin connector to allow hot plug capability. Integrated Tx and Rx signal conditioners provide high jitter-tolerance for full XFI compliance and no external reference clock required. The internally ac coupled high speed serial I/O simplifies interfacing to external circuitry. Dual 5V and 3.3V power supplies are needed. The optical output can be disabled by LVTTTL logic high-level input of TX_DIS. Loss of signal (RX_LOS) output is provided to indicate the loss of an input optical signal of receiver.

A serial EEPROM in the transceiver allows the user to access transceiver digital diagnostic monitoring and configuration data via the 2-wire XFP Management Interface. This interface uses a single address, A0h, with a memory map divided into a lower and upper area. Basic digital diagnostic data is held in the lower area while specific data is held in a series of tables in the high memory area.

ORDER INFORMATION

P/No.	Bit Rate (Gb/s)	10GBASE	Distance (km)	Wavelength (nm)	Package	Case Temp (°C)	RoHS Compliant
OPN-XH15-40LC2	9.95 – 10.5	ER/EW	40	1550 EML	XFP with DMI	0 to 70	Yes
OPN-XH15-40LC2I	9.95 – 10.5	ER/EW	40	1550 EML	XFP with DMI	-50 to 85	Yes

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	Tstg	-50	85	°C	
Operating Case Temperature	Topr	0	70	°C	OPN-XH15-40LC2
		-50	85		OPN-XH15-40LC2I
Relative Humidity	RH	0	85	%	Non condensing
Power Supply Voltage (5V)	Vcc5	-0.5	3.6	V	
Power Supply Voltage (3.3V)	Vcc3	-0.5	3.6	V	
Receiver Input Optical Power	Mip		4	dBm	Received average power

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Recommended Operating Conditions					
Parameter	Symbol	Min	Typ	Max	Units / Notes
Power Supply Voltage (5V)	V _{CC5}	4.75	5	5.25	V
Power Supply Voltage (3.3V)	V _{CC3}	3.13	3.3	3.47	V
Power Supply Current (@5V)	I _{CC5}			500	mA / 1
Power Supply Current (@3.3V)	I _{CC3}			750	mA / 1
Power Dissipation	P _D			3.5	W
Operating Case Temperature	T _{opr}	0		70	°C / OPN-XH15-40LC2
		-50		85	°C / OPN-XH15-40LC2I
Data Rate		9.95		10.5	Gb/s

1. Including in rush current. Maximum module current ramp rate is 100 mA/μs.

Transmitter Optical Specifications (T _{opr} = 0 to 70°C, V _{CC5} =5V±5%, V _{CC3} = 3.3V ±5%)						
Parameter	Symbol	Min	Typ	Max	Units	Notes
Average Launch Power	P _{O, Avg}	-4.7		4.0	dBm	2
Extinction Ratio	ER	3.0			dB	
Optical Modulation Amplitude	P _{O, OMA}	-1.7			dBm	2
Output Center Wavelength	λ _C	1530		1565	nm	
Output Spectrum Width	σ _λ			1	nm	-20 dB width
Side Mode Suppression Ratio	SMSR	30			dB	
Transmitter and Dispersion Penalty @ 800 ps/nm	TDP			3	dB	
Relative Intensity Noise	RIN			-130	dB/Hz	
Eye Mask	IEEE 802.3ae					
Average Launch Power of OFF Transmitter				-30	dBm	
Optical Return Loss Tolerance				21	dB	

2. Output power is power coupled into a 9/125 μm single-mode fiber.

Receiver Optical Specifications (T _{opr} = 0 to 70°C, V _{CC5} =5V±5%, V _{CC3} = 3.3V ±5%)						
Parameter	Symbol	Min	Typ	Max	Units	Notes
Sensitivity @ 10.3125 Gb/s	Sen1			-15.8	dBm	3
Receiver Overload	P _{MAX}	-1	---		dBm	
LOS -- Deasserted	LOS _D	---	---	-22	dBm	Transition: low to high
LOS -- Asserted	LOS _A	-28	---	---	dBm	Transition: high to low
LOS -- Hysteresis		0.5	---		dB	
Wavelength of Operation	λ _C	1260		1580	nm	
Optical Return Loss	ORL			-26	dB	

3. Average received power; Measured at 1530 to 1565 nm; BER < 10⁻¹² and PRBS 2³¹-1.

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Electrical Characteristics						
Parameter	Symbol	Min	Typ	Max	Units	Notes
High-Speed Signal (CML) Interface Specification						
Input Data Rate			9.95328 10.3125		Gb/s	4 5
Input Date Rate Tolerance			±20 ±100		ppm	4 5
Differential Input Impedance	R _{in}		100		Ω	
Differential Data Input Amplitude		120		820	mVpp	6, Internally AC coupled
Output Data Rate			9.95328 10.3125		Gb/s	4 5
Output Date Rate Tolerance			±100		ppm	4,5
Differential Output Impedance	R _{out}		100		Ω	
Differential Data Output Amplitude		340		850	mVpp	6, Internally AC coupled
Low-Speed Signal (LVTTTL) Interface Specification						
Input High Voltage		2.0		V _{cc}	V	
Input Low Voltage		GND		0.8	V	
Output High Voltage		2.4		V _{cc}	V	
Output Low Voltage		GND		0.5	V	
Reference Clock (LVPECL) Interface Specification						
No reference clock						

4. 10GBASE-EW.

5. 10GBASE-ER.

6. The differential input and output amplitudes are per XFP MSA mask at points B' and C'.

Transceiver Timing Characteristics						
Parameter	Symbol	Min	Typ	Max	Units	Notes
TX_DIS Assert Time	t _{off}			10	μs	
TX_DIS Negate Time	t _{on}			2	ms	
Time to Initialize	t _{init}			300	ms	
Interrupt Assert Delay	interrupt _{on}			200	ms	
Interrupt Negate Delay	interrupt _{off}			500	μs	
P_Down/PST Assert Delay	P_Down/RST _{on}			100	μs	
P_Down Nagate Delay	P_Down/RST _{off}			300	ms	
Mod_NR Assert Delay	Mod_nr _{on}			1	ms	
Mod_NR Negate Delay	Mod_nr _{off}			1	ms	
Mod_Desel Assert Time	T_Mod_Desel			2	ms	
Mod_Desel De-Assert Time	T_Mod_Sel			2	ms	
P_Down Reset Time	T _{reset}	10			μs	
RX_LOS Assert Delay	T_Los _{on}			100	μs	
RX_LOS Negate Delay	T_Los _{off}			100	μs	
Serial ID Clock Rate	f _{SCL}	0		400	kHz	

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Management Interface

The structure of the memory map is shown in Figure 1, which is accessible over a 2-wire serial interface at the 8-bit address 1010000X (A0h). The normal 256 byte I2C address space is divided into low and upper blocks of 128 Bytes. The lower block of 128 Bytes is always directly available and is used for the diagnostics and control function. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. Thus, there is a total available address space of 128*256 = 32 Kbytes in this upper memory space. The contents of Table 01h are listed in Table 1 below. Please refer SFF INF-8077i (Revision 4.5) for detailed information.

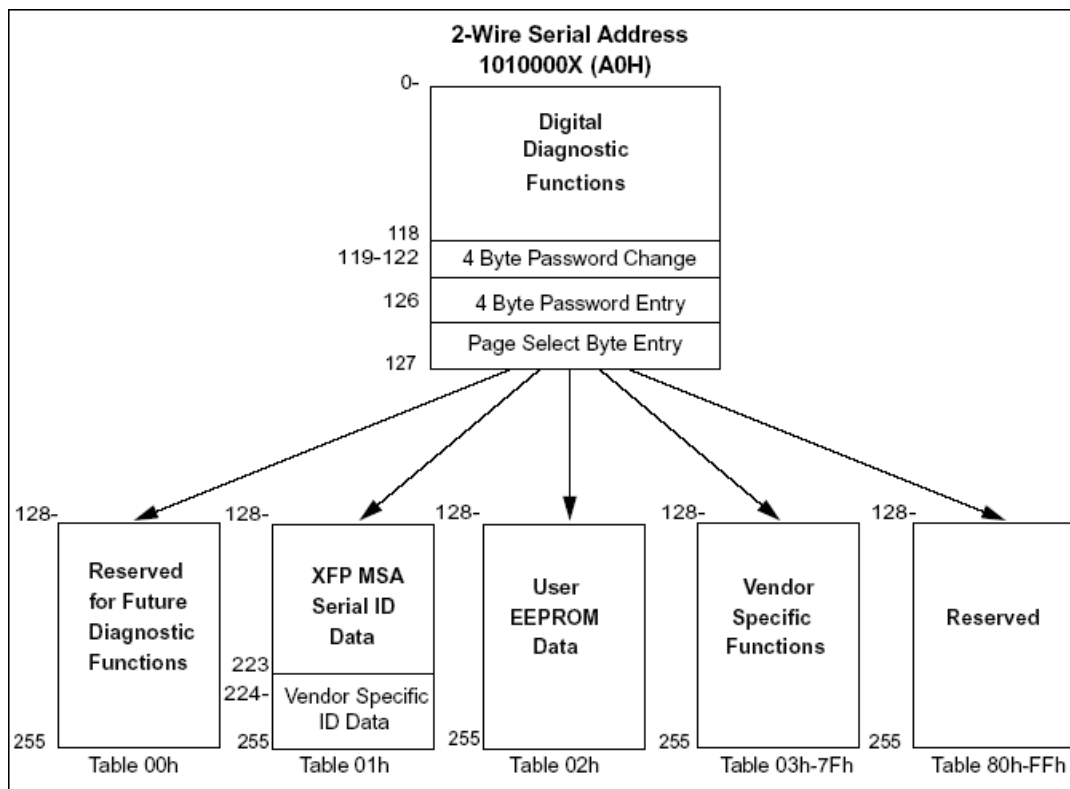


Figure 1. 2-wire Serial Digital Diagnostic Memory Map

Table 1 Monitoring Specification

Data Address	Parameter	Accuracy
96 ~ 97	Temperature	± 3°C
98 ~ 99	Reserved	
100 ~ 101	Tx Bias	± 10%
102 ~ 103	Tx Power	± 2dB
104 ~ 105	Rx Power	± 2dB
106 ~ 107	Vcc3	± 3%

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CONNECTION DIAGRAM

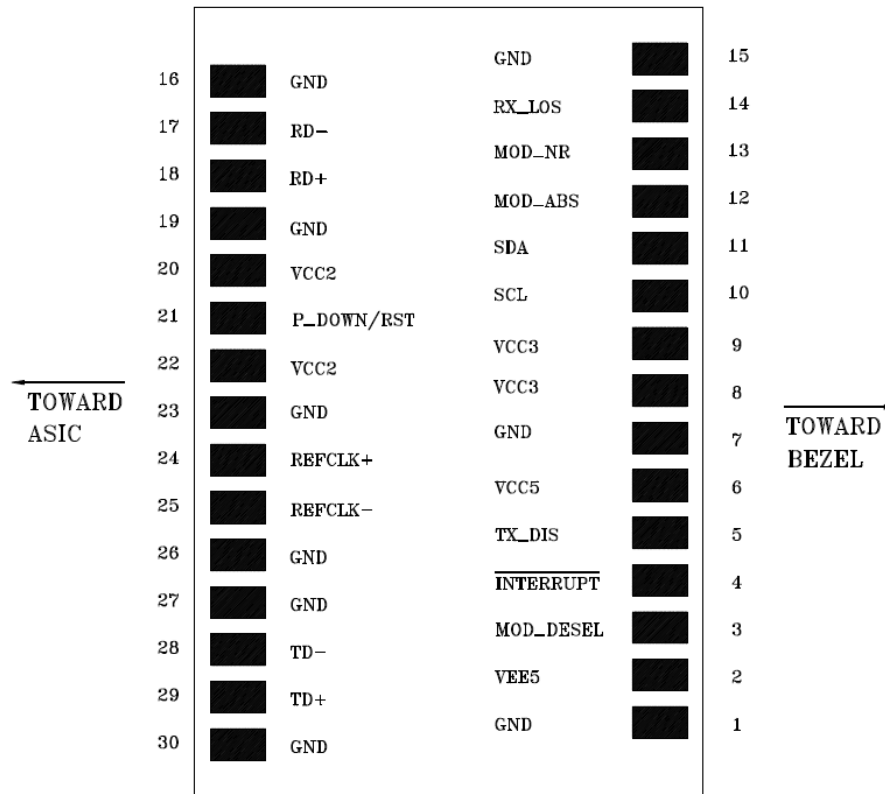


Table 3 PIN Description

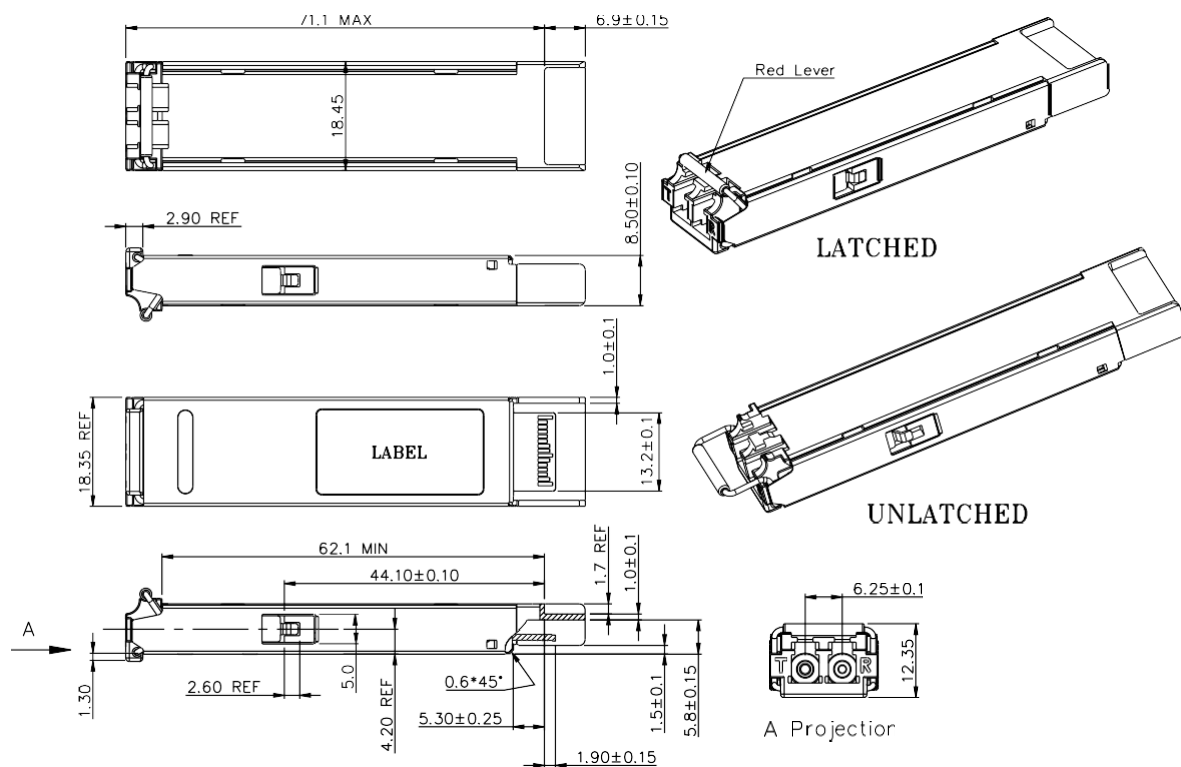
PIN	Logic	Signal Name	Description	Note
1		GND	Module Ground	1
2		VEE5	-5.2V Power Supply (Not required)	3
3	LVTTL-I	Mod_Desel	Module De-select; When held low allows module to respond to 2-wire serial interface	
4	LVTTL-O	Interrupt	Interrupt; Indicates presence of an important condition which can be read over the 2wire serial interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Turns off transmitter laser output	
6		VCC5	+5V Power Supply	3
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I/O	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Indicates Module is not present. Grounded in the Module	2
13	LVTTL-O	Mod_NR	Module Not Ready; Indicating Module Operational Fault	2
14	LVTTL-O	RX_LOS	Receiver Loss Of Signal Indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver Inverted Data Output	
18	CML-O	RD+	Receiver Non-Inverted Data Output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply (Not required)	3
21	LVTTL-I	P_Down/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode. Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	

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22		VCC2	+1.8V Power Supply (Not required)	3
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock Non-Inverted Input, AC coupled on the host board. (Not used. Internally terminated to 50 ohm (100 ohm diff.))	4
25	PECL-I	RefCLK-	Reference Clock Inverted Input, AC coupled on the host board. (Not used. Internally terminated to 50 ohm (100 ohm diff.))	4
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter Inverted Data Input	
29	CML-I	TD+	Transmitter Non-Inverted Data Input	
30		GND	Module Ground	1

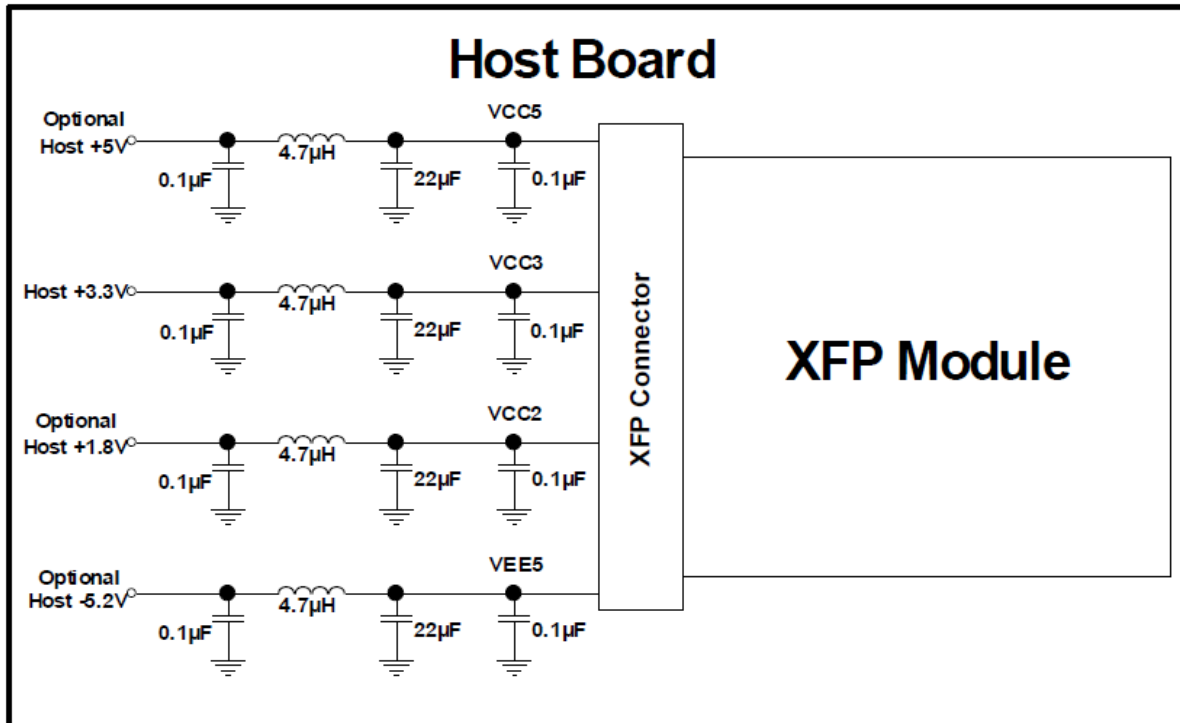
1. Module ground pins GND are isolated from the module case and chassis ground within the module.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.
3. These PINs are open within module.
4. A Reference Clock input is not required. If present, it will be ignored.

MECHANICAL SPECIFICATION (UNITS IN MM)



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RECOMMENDED POWER CIRCUIT SCHEMATIC



RECOMMENDED INTERFACE CIRCUIT

